SUPER FAMICOM DOCUMENTATION

SFX02

REGISTER (PPU)

A 1.000.000 BOYS A.K.A MEGABOYS PRODUCE

ADDRESS : 2100H
NAME : INIDISP
CONTENTS : INITIAL SETTINGS FOR SCREEN

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
BLANK-ING				FADE IN/OUT (0~15)			
				F3	F2	F1	F0

2 1 0 0 H

SCREEN BRIGHTNESS : Determine the Screen Brightness (16-Stages)

F3	F2	F1	F0	BRIGHTNESS
1	1	1	1	BRIGHT
1	1	1	0	¦
	\			¦
0	0	0	0	DARK

BLANKING : FORCED BLANKING
- 0 : NON-BLANKING
- 1 : BLANKING

ADDRESS : 2101H
NAME : OBJSEL
CONTENTS : OBJECT SIZE & OBJECT DATA AREA DESIGNATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
OBJ SIZE SELECT			OBJ NAME SELECT		OBJ NAME BASE SELECT		
S2	S1	S0	N1	N0	BA-2	BA-1	BA-0

2 1 0 1 H

OBJECT BASE ADDRESS (UPPER-3 BIT)
: Designate the segment (8K-word/segment) address which the OBJ data is stored in the VRAM (See Appendix-1 & 2)

OBJECT DATA AREA SELECT
: The upper 4K-word out of the area (8K-word) designated by "Object Base Address" is assigned as the Base Area. and the area of the lower 4K-word combined with its Base Area can be selected. (See Appendix-1 & 2)

OBJECT SIZE :DESIGNATE OBJECT SIZE (See Appendix-3 & 4)

S2	S1	S0	OBJ SIZE	
			0	1
0	0	0	8 DOT	16 DOT
0	0	1	8 DOT	32 DOT
0	1	0	8 DOT	64 DOT
0	1	1	16 DOT	32 DOT
1	0	0	16 DOT	64 DOT
1	0	1	32 DOT	64 DOT

(SIZE LARGE/SMALL)

ADDRESS : 2102H / 2103H
NAME : OAMADDL /OAMADDH
CONTENTS : ADDRESS FOR ACCESSING OAM (OBJECT ATTRIBUTE MEMORY)

ADDRESS

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
OAM ADDRESS								
A7	A6	A5	A4	A3	A2	A1	A0	2 1 0 2 H
OAM PRIORITY ROTATION							OAM ADDRESS MSB A8	2 1 0 3 H

- This is the INITIAL ADDRESS to be set in advance when reading from the OAM or writting to the OAM.

- By writing "1" to D7 (OAM Priority Rotation) of register <2103H> and setting the OAM address. the OBJ for the address set has highest priority.

- The address which has been set just before every field (beginning of V-BLANK) will be set again to registers <2102H> <2103H> automatically.
  But, the address can not be set automatically during Forced Blank period.

ADDRESS : 2104H
NAME : OAM DATA
CONTENTS : DATA FOR OAM WRITE

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
OAM DATA (LOW, HIGH)								
D7	D6	D5	D4	D3	D2	D1	D0	2 1 0 4 H

- This is the OAM data to be written at any address of the OAM. (See Appendix-3)

- After register <2102H> or <2103H> is accessed. the data must be written in the order of Lower 8-Bit & Upper 8-Bit of register <2104H>.
  The OAM address will be increased automatically when the OAM data is written in the order of LOW & HIGH.

- The data can be written only during V-BLANK or FORCED BLANK period.

ADDRESS : 2105H
NAME : BGMODE
CONTENTS : BG MODE & CHARACTER SIZE SETTINGS

D7	D6	D5	D4	D3	D2	D1	D0	
BG SIZE				BG3	BG MODE			2105H
BG 4	BG 3	BG 2	BG 1	PRIO.	M2	M1	M0	

BG SCREEN MODE SELECT : See BG Screen Mode Summary
(See Appendix-5)

HIGHEST PRIORITY DESIGNATION FOR BG-3 : Make BG3 highest priority
0 : OFF (See Appendix-16
1 : ON

BG SIZE DESIGNATION : Designate the size for each BG Character (See Appendix-18 & 19)
0 : 8 x 8 DOT/CHARACTER
1 : 16 x 16 DOT/CHARACTER

In case CHR NAME of SC data is "00H":

16 DOT × 16 DOT

00	01
10	11

CHARACTER NAME (HEX)

ADDRESS : 2106H
NAME : MOSAIC
CONTENTS : SIZE & SCREEN DESIGNATION FOR MOSAIC DISPLAY

D7	D6	D5	D4	D3	D2	D1	D0	
MOSAIC SIZE				MOSAIC ENABLE				2106H
M3	M2	M1	M0	BG 4	BG 3	BG 2	BG 1	

MOSAIC MODE SELECT : ON/OFF for Mosaic Mode of each BG
0 : OFF
1 : ON

MOSAIC MODE SIZE DESIGNATION : DESIGNATE MOSAIC MODE SIZE (SEE APPENDIX-6)

256 MODE

M3	M2	M1	M0	SIZE
0	0	0	0	1 x 1 DOT
0	0	0	1	2 x 2 DOT
0	0	1	0	3 x 3 DOT
	⋮			⋮
1	1	1	0	15x15 DOT
1	1	1	1	16x16 DOT

512 MODE H x V

M3	M2	M1	M0	SIZE ( ):NON-INTERLACE
0	0	0	0	2 x 2 DOT (2 x 1 DOT)
0	0	0	1	4 x 4 DOT (4 x 2 DOT)
0	0	1	0	6 x 6 DOT (6 x 3 DOT)
	⋮			
1	1	1	0	30×30 DOT (30×15 DOT)
1	1	1	1	32×32 DOT (32×16 DOT)

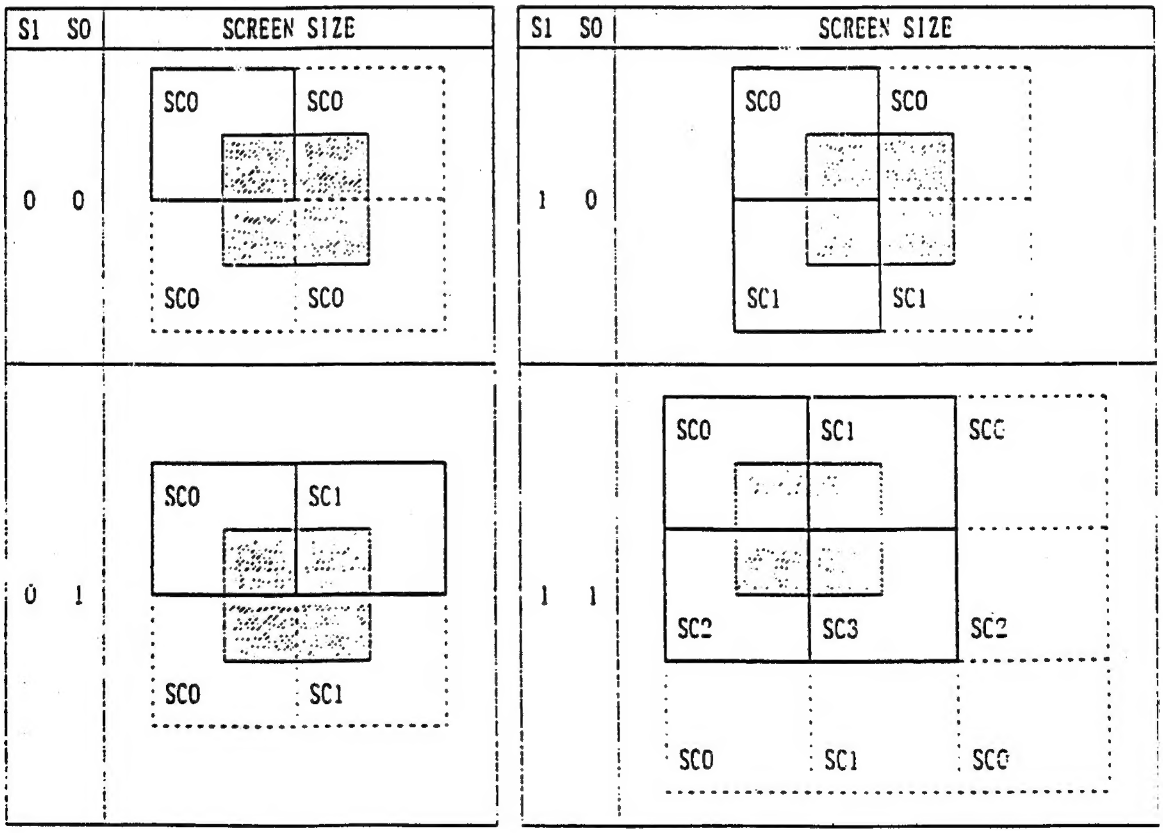
ADDRESS : 2107H / 2108H / 2109H / 210AH
NAME : BG1SC / BG2SC / BG3SC / BG4SC
CONTENTS : ADDRESS FOR STORING SC-DATA OF EACH BG & SC SIZE DESIGNATION (MODE 0 ~3)

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
BG1 SC BASE ADDRESS						BG1 SC SIZE		2107H
A5	A4	A3	A2	A1	A0	S1	S0	
BG2 SC BASE ADDRESS						BG2 SC SIZE		2108H
A5	A4	A3	A2	A1	A0	S1	S0	
BG3 SC BASE ADDRESS						BG3 SC SIZE		2109H
A5	A4	A3	A2	A1	A0	S1	S0	
BG4 SC BASE ADDRESS						BG4 SC SIZE		210AH
A5	A4	A3	A2	A1	A0	S1	S0	

SCREEN SIZE DESIGNATION (See Appendix-18 & 19)
: Designate Background Screen Size

BACKGROUND SCREEN BASE ADDRESS (UPPER 6-BIT)
: Designate the segment which BG-SC data in the VRAM is stored.
(1K-WORD/SEGMENT)

SCREEN SIZE & SCREEN REPETITION



ADDRESS : 210BH / 210CH
NAME : BG12NBA / BG34NBA
CONTENTS : BG CHARACTER DATA AREA DESIGNATION

D7	D6	D5	D4	D3	D2	D1	D0	
BG2 NAME BASE ADDRESS				BG1 NAME BASE ADDRESS				210BH
A3	A2	A1	A0	A3	A2	A1	A0	

D7	D6	D5	D4	D3	D2	D1	D0	
BG4 NAME BASE ADDRESS				BG3 NAME BASE ADDRESS				210CH
A3	A2	A1	A0	A3	A2	A1	A0	

BACKGROUND NAME BASE ADDRESS (UPPER 4-BIT)
: Designate the segment address in the VRAM which BG character data is stored.
(4K-WORD/SEGMENT)

ADDRESS : 210DH / 210EH
NAME : BG1HOFS / BG1VOFS
CONTENTS : H/V SCROLL VALUE DESIGNATION FOR BG-1

D7	D6	D5	D4	D3	D2	D1	D0	
BG1 H-OFFSET (LOW, HIGH)								210DH
			(HO12)	(HO11)	(HO10)	(HO 9)	(HO 8)	
HO 7	HO 6	HO 5	HO 4	HO 3	HO 2	HO 1	HO 0	

D7	D6	D5	D4	D3	D2	D1	D0	
BG1 V-OFFSET (LOW, HIGH)								210EH
			(VO12)	(VO11)	(VO10)	(VO 9)	(VO 8)	
VO 7	VO 6	VO 5	VO 4	VO 3	VO 2	VO 1	VO 0	

- 10-Bit maximum (0 ~ 1023) can be designated for H/V scroll value.
  [The size of 13-bit maximum (-4096~4095) can be designated in MODE-7] (See Appendix-8 & 9)

- By writing to the register twice, the data can be set in the order of Low and High.

ADDRESS : 210F H / 2110 H / 2111 H / 2112 H / 2113 H / 2114 H
NAME : BG2HOFS / BG2VOFS / BG3HOFS / BG3VOFS / BG4HOFS / BG4VOFS
CONTENTS : H/V SCROLL VALUE DESIGNATION FOR BG-2, 3, 4

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
'BG 'H-OFFSET (LOW, HIGH)'								210FH
						(HO 9)	(HO 8)	2111H
HO 7	HO 6	HO 5	HO 4	HO 3	HO 2	HO 1	HO 0	2113H

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
'BG 'V-OFFSET (LOW, HIGH)'								2110H
						(VO 9)	(VO 8)	2112H
VO 7	VO 6	VO 5	VO 4	VO 3	VO 2	VO 1	VO 0	2114H

- 10 bit maximum (0~1023) of the H/V scroll value can be designated. (See Appendix-8)

- By writing to the register twice, the data can be set in the order of Low and High.

ADDRESS : 2115H
NAME : VMAINC
CONTENTS : VRAM ADDRESS INCREMENT VALUE DESIGNATION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
H/L				V-RAM ADDRESS SEQUENCE MODE				210BH
				FULL GRAPHIC		SC INCREMENT		
INC				G1	G0	I1	I0	

Designate the increment value for the VRAM address
(See Appendix-7)

G1	G0	I1	I0	INCREMENT VALUE
0	1	0	0	Increment by 8 for 32 times (2-Bit Formation)
1	0	0	0	Increment by 8 for 64 times (4-Bit Formation)
1	1	0	0	Increment by 8 for 128 times (8-Bit Formation)
0	0	0	0	Address Increments 1 BY 1
0	0	0	1	Address Increments 32 BY 32
0	0	1	0	Address Increments 64 BY 64
0	0	1	1	Address Increments 128 BY 128

Designate the increment timing for the address

0 : The address will be increased after the data has been written to register <2118H> or the data has been read from register <2139H>.

1 : The address will be increased after the data has been written to register <2119H> or the data has been read from register <213AH>.

ADDRESS : 2116H / 2117H
NAME : VMADDL / VMADDH
CONTENTS : ADDRESS FOR VRAM READ

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
VRAM ADDRESS (LOW)								2 1 1 6 H
A7	A6	A5	A4	A3	A2	A1	A0	
VRAM ADDRESS (HIGH)								2 1 1 7 H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is the initial address for reading from the VRAM or writing to the VRAM.
- The data is read or written by the address set initially. and every time the data is read. the address will be increased automatically.
- The value to be increased is determined by "SC INCREMENT" of register <2115H> and the setting value of the "FULL GRAPHIC".

ADDRESS : 2118H / 2119H
NAME : VMDATAL / VMDATAH
CONTENTS : DATA FOR VRAM WRITE

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
VRAM DATA (LOW)								2 1 1 8 H
A7	A6	A5	A4	A3	A2	A1	A0	
VRAM DATA (HIGH)								2 1 1 9 H
A15	A14	A13	A12	A11	A10	A9	A8	

- This is the screen data and character data (BG & OBJ). which can write at any address of the VRAM
- According to the settings of register <2115H> "H/L INC". the data can be written to the VRAM as follows:

H/L INC	WRITE TO REGISTER	OPERATION
0	Write to <2118H> only	The Data is written to lower 8-bit of the VRAM and the address will be increased automatically.
1	Write to <2119H> only	The Data is written to upper 8-bit of the VRAM and the address will be increased automatically.
0	Write in the order of <2119H> & <2118H>	When the data is set in the order of upper & lower the address will be increased.
1	Write in the order of <2118H> & <2119H>	When the data is set in the order of lower & upper the address will be increased.

NOTE : The data can be written only during V-BLANK or FORCED BLANK period.

ADDRESS : 211AH
NAME : M7SEL
CONTENTS : INITIAL SETTING IN SCREEN MODE-7

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
SCREEN OVER						SCREEN FLIP	
01	00					V	H

2 1 1 AH

HORIZONTAL/VERTICAL FLIP
: H-FLIP/V-FLIP in the Screen Mode-7

V	H	DISPLAY
0	0	Normal display
0	1	H-Directional Flip only
1	0	V-Directional Flip only
1	1	Both H & V Directional Flip

The following process is made if the screen to be displayed is outside of the screen area.

01	00	PROCESS OUT OF AREA
0	0	Screen repetition if outside of screen area
1	0	Character # repetition if outside of screen area
1	1	Outside of the screen area is the Back Drop Screen in single color

ADDRESS : 211B H / 211C H / 211D H / 211E H / 211F H / 2120 H
NAME : M7A / M7B / M7C / M7D / M7X / M7Y
CONTENTS : ROTATION/ENLARGEMENT/REDUCTION IN MODE-7, CENTER COORDINATE SETTINGS & MULTIPLICAND/MULTIPLIER SETTINGS OF COMPLEMENTARY MULTIPLICATION

D7	D6	D5	D4	D3	D2	D1	D0	
MATRIX PARAMETER A (LOW, HIGH)								211BH
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER B (LOW, HIGH)								211CH
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER C (LOW, HIGH)								211DH
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	
MATRIX PARAMETER D (LOW, HIGH)								211EH
(MP15)	(MP14)	(MP13)	(MP12)	(MP11)	(MP10)	(MP 9)	(MP 8)	
MP 7	MP 6	MP 5	MP 4	MP 3	MP 2	MP 1	MP 0	

- The 8-bit data should be written twice in the order of lower and upper. Then, the parameter of rotation, enlargement and reduction should be set by its 16-bit data.
- The value down to a decimal point should be set to the lower 8-bit. The most significant bit of the upper 8-bit is for the signed bit. (MP15 is the signed bit. There is a decimal point between M7 & M8
- FORMULA FOR ROTAION/ENLARGEMENT/REDUCTION (See Appendix-13)

$$\begin{pmatrix} X_2 \\ Y_2 \end{pmatrix} = \begin{pmatrix} A & B \\ C & D \end{pmatrix} \begin{pmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{pmatrix} + \begin{pmatrix} X_0 \\ Y_0 \end{pmatrix}$$

$A=\cos\gamma\times(1/\alpha)$, $B=\sin\gamma\times(1/\alpha)$, $C=-\sin\gamma\times(1/\beta)$, $D=\cos\gamma\times(1/\beta)$

γ : Rotation Angle α : Reduction Rates for X(H) β : Reduction Rates for Y(V)

$X_0 \cdot Y_0$: Center Coordinate. $X_1 \cdot Y_1$: Display Coordinate.

$X_2 \cdot Y_2$: Coordinate before Calculation

- Set the value of " A" to the register <211BH>. In the same way, set "B~D" to the register <211CH> ~<211EH>.

* The complementary multiplication (16-bit x 8-bit) can be done by using regidters <211BH> <211CH>. When setting 16-bit data to register <211BH> and 8-bit data to register <211CH>, the multiplication result can be indicated rapidly by reading registers <2134H> ~<2136H>.

d7	d6	d5	d4	d3	d2	d1	d0	
CENTER POSITION X_0 (LOW, HIGH)								211FH
			(X12)	(X11)	(X10)	(X9)	(X8)	
X7	X6	X5	X4	X3	X2	X1	X0	
CENTER POSITION Y_0 (LOW, HIGH)								2120H
			(Y12)	(Y11)	(Y10)	(Y9)	(Y8)	
Y7	Y6	Y5	Y4	Y3	Y2	Y1	Y0	

- The center coordinate (X_0, Y_0) for Rotation/Enlargement/Reduction can be designated by this register.
- The coordinate value of X_0 & Y_0 can be designated by 13-bit (complement of 2).
- This register requires that the lower 8-bit is set first and the upper 8-bit is set. Therefore, 13-bit data in total can be set.

ADDRESS : 2121H
NAME : CGADD
CONTENTS : ADDRESS FOR CG-RAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0
CG RAM ADDRESS							
A7	A6	A5	A4	A3	A2	A1	A0

2121H

- This is the initial address for reading from the CG-RAM or writing to the CG-RAM
- The data is read by the address set initially, and every time the data is read or written, the address will be increased automatically.

ADDRESS : 2122H
NAME : CGDATA
CONTENTS : DATA FOR CG-RAM WRITE

D7	D6	D5	D4	D3	D2	D1	D0
	CG RAM DATA (LOW, HIGH)						
	(D14)	(D13)	(D12)	(D11)	(D10)	(D9)	(D8)
D7	D6	D5	D4	D3	D2	D1	D0

2122H

- This is the color generater data to be written at any address of the CG-RAM.
- The mapping of BG1～BG4 and OBJ data in the CG-RAM will be determined, which is performed by every mode selected by "BG MODE" of register <2105H>. (See Appendix-14)
- There are the color data of 8-palettes for each screen of BG1 ～ BG4. The palette selection is determined by 3-bit of the SC data "COLOR".
- Because the CG-RAM data is 15-bit/word, it is necessary to set lower 8-bit first to this register and then upper 7-bit should be set.
  When both lower and upper are set, the address will be increased by 1 automatically.

NOTE : After the address is set, the data should be written from the lower as well as the OAM.

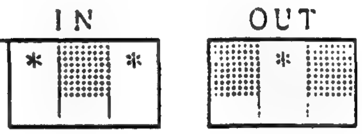
NOTE : The data can be written only during H/V BLANK or FORCED BLANK period.

ADDRESS : 2123H / 2124H / 2125H
NAME : W12SEL / W34SEL / WOBJSEL
CONTENTS : WINDOW MASK SETTINGS (BG1~ BG4. OBJ. COLOR)

D7	D6	D5	D4	D3	D2	D1	D0	
BG2 WINDOW				BG1 WINDOW				2123H
W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT	
BG4 WINDOW				BG3 WINDOW				2124H
W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT	
COLOR WINDOW				OBJ WINDOW				2125H
W2 EN	IN/OUT	W1 EN	IN/OUT	W2 EN	IN/OUT	W1 EN	IN/OUT	

WINDOW IN/OUT : The window mask area can be designated whether inside or outside of the frame designated by the window position.

0 : IN
1 : OUT



*: DISPLAY AREA

WINDOW-1 ENABLE : Window-1 ON/OFF Designation
WINDOW-2 ENABLE : Window-2 ON/OFF Designation

0 : OFF
1 : ON

The COLOR WINDOW is a window for main and sub screen. (It is related to the register <2130H>)

ADDRESS : 2126H / 2127H / 2128H / 2129H
NAME : WH0 / WH1 / WH2 / WH3
CONTENTS : WINDOW POSITION DESIGNATION (SEE APPENDIX-15)

D7	D6	D5	D4	D3	D2	D1	D0
WINDOW H0/H1/H2/H3 PPOSITION							
P7	P6	P5	P4	P3	P2	P1	P0

2126H WINDOW-1 LEFT POSITION
2127H DESIGNATION
2128H
2129H

WINDOW H0 POSITION <2126H> : Window-1 Left Position Designation. It can be set in range of 0 ~ 255.

WINDOW H1 POSITION <2127H> : Window-1 Right Position Designation. It can be set in range of 0 ~ 255.

WINDOW H2 POSITION <2128H> : Window-2 Left Position Designation. It can be set in range of 0 ~ 255.

WINDOW H3 POSITION <2129H> : Window-2 Right Position Designation. It can be set in range of 0 ~ 255.

NOTE : If "LEFT POSITION SETTING VALUE> RIGHT POSITION SETTING VALUE" is assumed.
there will be no range of the window.

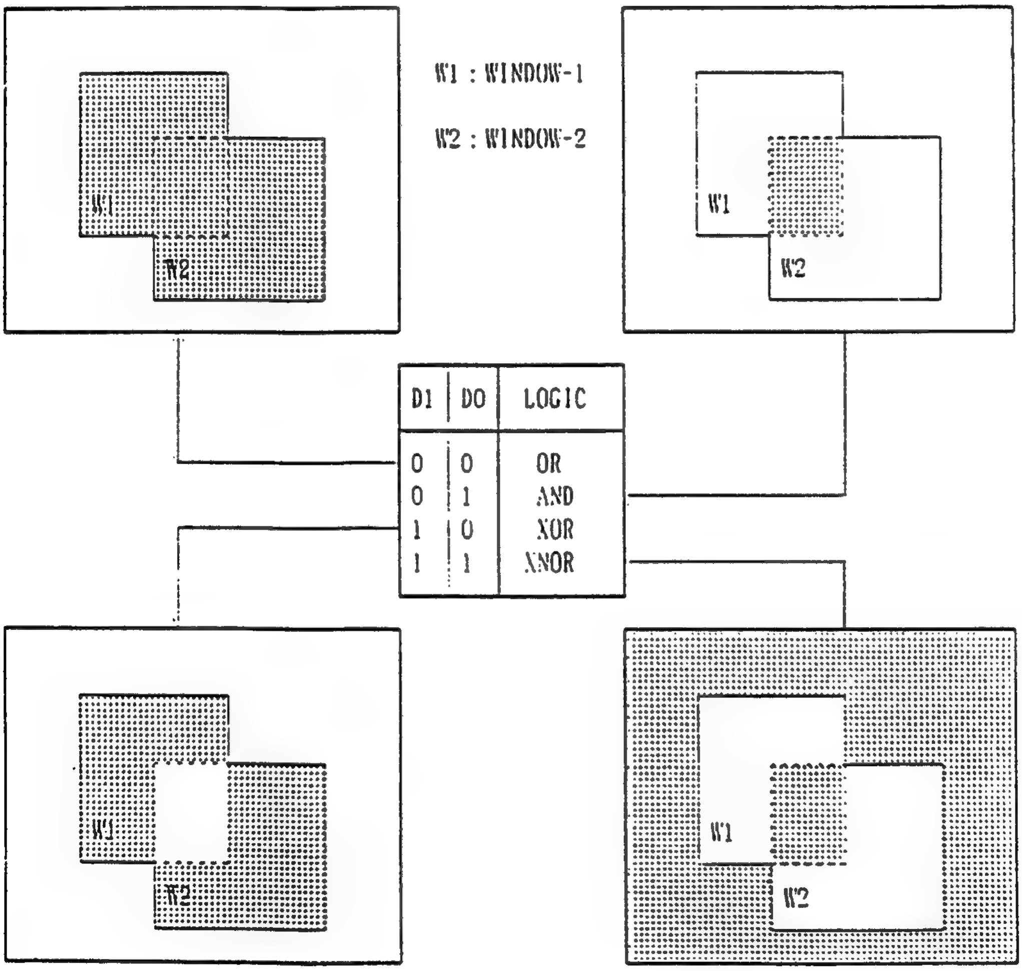
ADDRESS : 212AH / 212BH
NAME : WBGLOG / WOBJLOG
CONTENTS : MASK LOGIC SETTINGS FOR WINDOW-1 & 2 ON EACH SCREEN

D7	D6	D5	D4	D3	D2	D1	D0	
WINDOW LOGIC								212AH
BG4		BG3		BG2		BG1		
D1	D0	D1	D0	D1	D0	D1	D0	

D7	D6	D5	D4	D3	D2	D1	D0	
				WINDOW LOGIC				212BH
				Color		OBJ		
				D1	D0	D1	D0	

WINDOW LOGIC : SET MASK LOGIC FOR WINDOW-1 & 2

When both window-1 and window-2 are "IN", the shaded portion will be masked as follows:



D1	D0	LOGIC
0	0	OR
0	1	AND
1	0	XOR
1	1	XNOR

NOTE : "IN/OUT" of registers <2123H> <2124H> <2125H> becomes the "NOT logic" for each window-1 and window-2.

ADDRESS : 212CH
NAME : TM
CONTENTS : MAIN SCREEN DESIGNATION

D7	D6	D5	D4	D3	D2	D1	D0
			THROUGH MAIN				
			OBJ	BG 4	BG 3	BG 2	BG 1

2 1 2 CH

MAIN SCREEN DESIGNATION
: Designate the screen (BG1 ~ BG4, OBJ) to be displayed as the Main Screen.
Designate the screen to be added for the screen addition/subtraction
0 : DISABLE
1 : ENABLE

ADDRESS : 212DH
NAME : TS
CONTENTS : SUB SCREEN DESIGNATION

D7	D6	D5	D4	D3	D2	D1	D0
			THROUGH SUB				
			OBJ	BG 4	BG 3	BG 2	BG 1

2 1 2 DH

SUB SCREEN DESIGNATION
: Designate the screen (BG1 ~ BG4, OBJ) to be displayed as SUB-Screen.
Designate the addition/subtraction screen at the point when the screen addition/subtraction is functioning.
0 : DISABLE
1 : ENABLE

※ When the screen addition/subtraction is functioning, the SUB screen is a screen to be added or subtracted against the MAIN screen.

ADDRESS : 212EH
NAME : TMW
CONTENTS : WINDOW MASK DESIGNATION FOR MAIN SCREEN

D7	D6	D5	D4	D3	D2	D1	D0
			THROUGH MAIN (WINDOW)				
			OBJ	BG 4	BG 3	BG 2	BG 1

2 1 2 E H

WINDOW MASK DESIGNATION FOR MAIN SCREEN
: In the window area designated by register <2123H> ~ <2129H>, the screen to be displayed can be designated, which is selected among the Main screen designated by register <212CH>.

0 : DISABLE
1 : ENABLE

ADDRESS : 212FH
NAME : TSW
CONTENTS : WINDOW MASK DESIGNATION FOR SUB SCREEN

D7	D6	D5	D4	D3	D2	D1	D0
			THROUGH SUB (WINDOW)				
			OBJ	BG 4	BG 3	BG 2	BG 1

2 1 2 F H

WINDOW MASK DESIGNATION FOR SUB SCREEN
: In the window area designated by register <2123H> ~ <2129H>, the screen to be displayed can be designated, which is selected among the Sub screen designated by register <212CH>.

0 : DISABLE
1 : ENABLE

※ When the screen addition subtraction is functioning, the SUB screen is a screen to be added or subtracted against the MAIN screen.

ADDRESS : 2130H
NAME : CGSWSEL
CONTENTS : INITIAL SETTINGS FOR FIXED COLOR ADDITION OR SCREEN ADDITION

D7	D6	D5	D4	D3	D2	D1	D0	
COLOR WINDOW ON/OFF						CC ADD	DIRECT	2130H
MAIN SW (A)		SUB SW (B)						
M1	M0	S1	S0			ENABLE	SELECT	

DIRECT SELECT (See Appendix-14)
: The VRAM data (Color and Character data) become the color data directly. (Only when mode-3, 4 & 7 are selected
0 : DISABLE
1 : ENABLE

COLOR WINDOW ON/OFF MAIN/SUB SWITCH
: When the Color Window is functioning, the assignment of the window area for MAIN and SUB screen can be designated.

FIXED COLOR ADDITION/SUBTRACTION ENABLE
: Designate whether 2 kinds of the data should be added/subtracted each other or not, which are the fixed color set by register <2132H> and the color data which is set to the CGRAM.
0 : ADDITION/SUBTRACTION FOR FIXED COLOR
1 : ADDITION/SUBTRACTION FOR SUB SCREEN

M1(S1)	M0(S0)	FUNCTION
0	0	ON (All the time)
0	1	ON (inside window only)
1	0	ON (outside window only)
1	1	OFF (All the time)

ADDRESS : 2131H
NAME : CGADSUB
CONTENTS : ADDITION/SUBTRACTION & SUBTRACTION DESIGNATION FOR EACH SCREEN, OBJ & BACKGROUND COLOR

D7	D6	D5	D4	D3	D2	D1	D0	
ADD	1/2	ADD or SUB ENABLE						2131H
SUB	ENABLE	BACK	OBJ	BG 4	BG 3	BG 2	BG 1	

COLOR DATA ADDITION/SUBTRACTION ENABLE
: Designate the selection either of the disable or the enable for the addition/subtraction of the fixed color data or the screen color data.
0 : DISABLE
1 : ENABLE (Addition/Subtraction function : ON

NOTE : In case the OBJ is designated, the Addition Subtraction function is available only when the OBJ color palette is either 6 or 7.

"½ OF COLOR DATA" DESIGNATION : When the color constant addition/subtraction or the screen addition/subtraction is performed, designate whether the RGB result in the addition/subtraction area should be "½" or not. However, in the back (color constant) area on the Sub screen, it does not become "½".
0 : DISABLE
1 : ENABLE (½ function : ON)

COLOR DATA ADDITION/SUBTRACTION SELECT: Designate the selection either of the addition or the subtraction mode.
0 : ADDITION MODE SELECT
1 : SUBTRACTION MODE SELECT

ADDRESS : 2132H
NAME : COLDATA
CONTENTS : FIXED COLOR DATA FOR FIXED COLOR ADDITION/SUBTRACTION

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
COLOR CONSTANT DATA							
			COLOR BRILLIANCE DATA				
BLUE	GREEN	RED	D4	D3	D2	D1	D0

2 1 3 2 H

COLOR CONSTANTOR DATA : Set the color constant data for color constant addition/subtraction

COLOR DESIGNATION : BIT FOR SELECTING DESIRED COLOR

- R/G/B brightness should be set by the data of each 5-Bit.

(EXAMPLE) RED : C0H, 3FH (B=00H, G=00H, R=1FH)
GREEN : A0H, 5FH (B=00H, G=1FH, R=00H)
BLUE : 60H, 9FH (B=1FH, G=00H, R=00H)
WHITE : FFH
BLACK : E0H

ADDRESS : 2133H
NAME : SETINI
CONTENTS : SCREEN INITIAL SETTING

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0
EXT. SYNC.	EXT. INPUT			PSEUDO 5 1 2	224/239	OBJ-V SELECT	INTER-LACE

2 1 3 3 H

SCANNING : INTERLACE/NON-INTERLACE SELECTION
(It relates to <2105H>.)
0 : NON-INTERLACE
1 : INTERLACE

OBJ V-DIRECTION DISPLAY
: In the interlace mode, select either of 1-dot per line or 1-dot repeated every 2 lines. If "1" is written, the OBJ seems to be reduced half vertically in appearance.

(If "1" is set other than the interlace mode, even-numbered line and odd-numbered line of the OBJ will be dusplayed alternately every field.)

BG V-DIRECTION DISPLAY :Switch the display line of a field to 224-Line or 239-Line.
(In case of interlace mode, it will be doubled dot.)
0 : 224 LINE
1 : 239 LINE

HORIZONTAL PSEUDO 512 MODE : 512 imaginary resolution (Horizontal) can be made by shifting the SUB screen half dot to the left.
alternately every field
0 : DISABLE
1 : ENABLE

EXTBG MODE (SCREEN EXPAND): Enable the data supplied from the external LSI. For the SFX, enable when the screen with priority is used on mode-7.

EXTERNAL SYNCHRONIZATION : It is used for super-impose and etc. Normally, "0" should be written.

ADDRESS : 2134H / 2135H / 2136H
NAME : *MPYL / *MPYM / *MPYH
CONTENTS : MULTIPLICATION RESULT

D7	D6	D5	D4	D3	D2	D1	D0	
MPY (LOW)								2134H
M7	M6	M5	M4	M3	M2	M1	M0	

D7	D6	D5	D4	D3	D2	D1	D0	
MPY (MID)								2135H
M15	M14	M13	M12	M11	M10	M9	M8	

D7	D6	D5	D4	D3	D2	D1	D0	
MPY (HIGH)								2136H
M23	M22	M21	M20	M19	M18	M17	M16	

- This is a Multiplication result (complement of 2) can be read by setting 16-bit to register <211BH> and setting 8-Bit data to register <211CH>.

ADDRESS : 2137H
NAME : *SLHV
CONTENTS : SOFTWARE LATCH FOR H/V COUNTER

D7	D6	D5	D4	D3	D2	D1	D0	
SOFT LATCH FOR H/V COUNTER								2137H
SL7	SL6	SL5	SL4	SL3	SL2	SL1	SL0	

- This is a register, which generate the pulse for latching the H/V counter value.
- The H/V counter value at the point when register <2137H> is read can be latched. The data which was read is meaningless data.
- The H/V counter value latched can be reffered by registers <213CH> <213DH>.

ADDRESS : 2138H
NAME : *OAMDATA
CONTENTS : READ DATA FROM OAM

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
OAM DATA (LOW, HIGH)								2138H
D7	D6	D5	D4	D3	D2	D1	D0	

- This is a register, which can read the data at any address of the OAM.

- When the address is set to register <2102H><2103H> and register <2138H> is also accessed, the data can be read in the order of Low 8-bit/High 8-bit.
  Afterward, the address will be increased automatically, and the data of the next address can be read.

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

ADDRESS : 2139H / 213AH
NAME : *VMDATAL / *VMDATAH
CONTENTS : READ DATA FROM VRAM

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
VRAM DATA (LOW)								2139H
D7	D6	D5	D4	D3	D2	D1	D0	

VRAM DATA (HIGH)								213AH
D15	D14	D13	D12	D11	D10	D9	D8	

- This is a register, which can read the data at any address of the VRAM.

- The initial address should be set by registers <2116H> and <2117H>. The data can be read by the address which has been set initially.

- When reading the data continuously, the first data for the address increment should be read as a dummy data after the address has been set.

- Quantity to be increased will be determined by "SC INCREMENT" of register <2115H> and the setting value of the "FULL GRAPHIC"

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

ADDRESS : 213BH
NAME : *CGDATA
CONTENTS : READ DATA FROM CG-RAM

D7	D6	D5	D4	D3	D2	D1	D0	
	CG DATA (LOW, HIGH)							213BH
	(D14)	(D13)	(D12)	(D11)	(D10)	(D9)	(D8)	
D7	D6	D5	D4	D3	D2	D1	D0	

- This is a register. which can read the data at any address of the CG-RAM.

- The initial address can be set by register <2121H>. The lower 8-bit is read first. and then the upper 7-bit will be read by accessing this register.
  The current address will be increased to the next address at the same time the upper 7-bit is read.

NOTE : The data can be read only during H/V BLANK or FORCED BLANK period.

ADDRESS : 213CH / 213DH
NAME : *OPHCT / *OPVCT
CONTENTS : H/V COUNTER DATA BY EXTERNAL OR SOFTWARE LATCH

D7	D6	D5	D4	D3	D2	D1	D0	
	OUTPUT DATA OF H-COUNTER							213CH
							(H8)	
H7	H6	H5	H4	H3	H2	H1	H0	
	OUTPUT DATA OF V-COUNTER							213DH
							(V8)	
V7	V6	V5	V4	V3	V2	V1	V0	

- The H/V counter is latched by reading register <2137H>. and its H/V counter value can be read by this register.

- The H/V counter is also latched by the external latch. and its value can be read by this register.

- If register <213CH> or <213DH> is read after register <213FH> has been read. the lower 8-bit data will be read first. and then the upper 1-bit will be read by reading the register.

ADDRESS : 213EH
NAME : *STAT77
CONTENTS : PPU STATUS FLAG & VERSION NUMBER

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
TIME OVER	RANGE OVER	MASTER /SLAVE		5 C 7 7 VERSION NUMBER				2 1 3 E H

MASTER / SLAVE MODE SELECT : LSI MODE (Normally "0" is set)

OBJ DISPLAY STATUS (ON A HORIZONTAL LINE)
- RANGE : When Quantity of the OBJ (regardless of the size) becomes 33 pcs or more. "1" will be set.
- TIME : When quantity of the OBJ which is converted to "8 X 8-SIZE" is 35 pcs or more. "1" will be set.

NOTE : The flag will be reset at the end of the V-BLANK period.

ADDRESS : 213FH
NAME : *STAT78
CONTENTS : PPU STATUS FLAG & VERSION NUMBER

D 7	D 6	D 5	D 4	D 3	D 2	D 1	D 0	
FIELD	EXT. LATCH		NTSC/PAL	5 C 7 8 VERSION NUMBER				2 1 3 F H

DISPLAY METHOD
- 0 : NTSC
- 1 : PAL

EXTERNAL LATCH FLAG : When the external signal (Light Pen. etc.) is applied. it enables to latch the H/V counter value.

FIELD : This is a status flag. which indicates whether 1st field is scanned or 2nd field is scanned the interlace mode. (The definition is different from the field of NTSC)
- 0 : 1ST FIELD
- 1 : 2ND FIELD

- When this register is read. registers <213CH> <213DH> will be initialized individually in the order of Low and High.

ADDRESS : 2140H / 2141H / 2142H / 2143H
NAME : APUIO0 / APUIO1 / APUIO2 / APUIO3
CONTENTS : COMMUNICATION PORT WITH APU

D7	D6	D5	D4	D3	D2	D1	D0	
APU I/O PORT								2140H 2141H 2142H 2143H

- This port provides more registers for the purpose of IN/OUT, which are 8 registers in total in the APU.
  Therehore, the different register will be accessed, whether reading or writing for the same address.

- See APU MANUAL for the details of the communication method

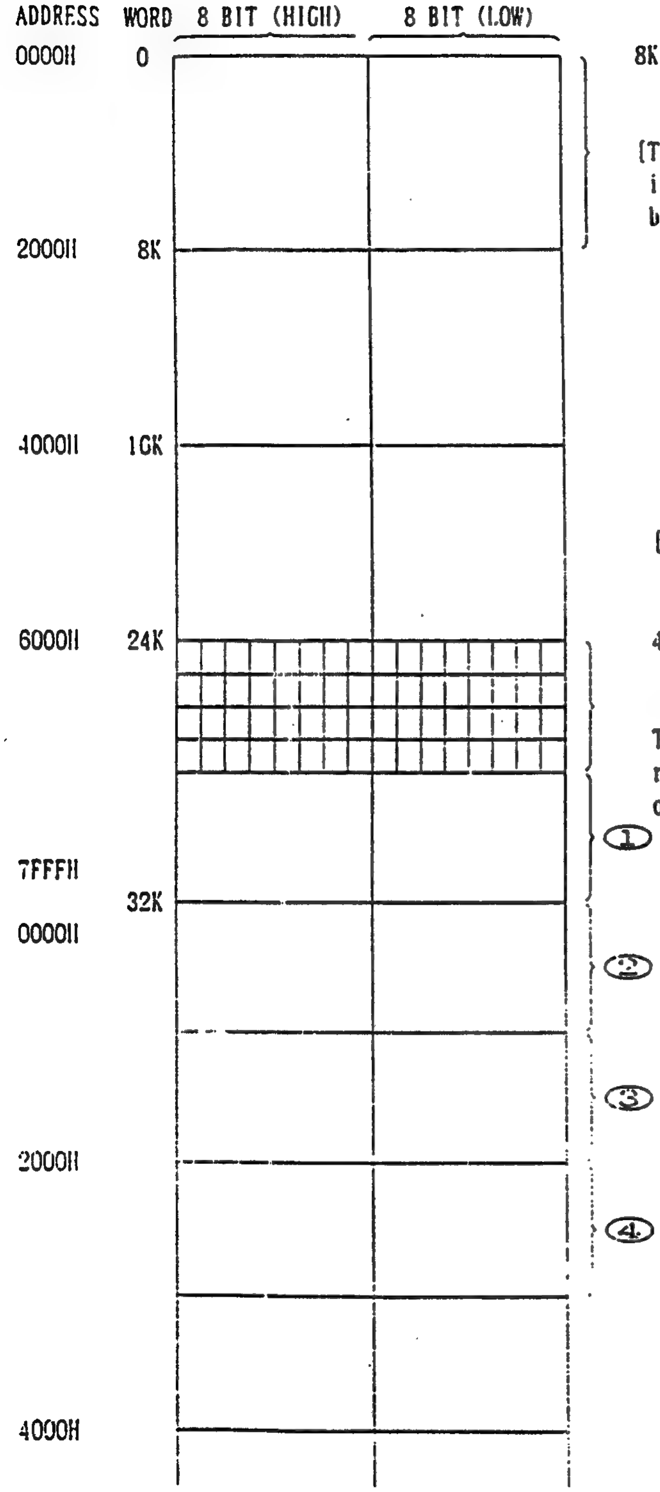
SUPER FAMICOM DOCUMENTATION

SFX02X

REGISTER (PPU)

APPENDIX

A 1.000.000 BOYS A.K.A MEGABOYS PRODUCE



8K-WORD : This is a area which is designated by "OBJ NAME BASE ADDRESS" of the register <2101H>.
(32K-WORD / 4-Partitio
[The BA2 of the register <2101H> "OBJ NAME BASE ADDRES is used for expansion purpose, and it will normally be ignored.]

[In case BA1=1 and BA0=1 are set by "OBJ NAME BASE ADDRESS"

4K-WORD :This is a lower 4K-WORD of the area (8K-WOR designated by "OBJ NAME BASE ADDRESS" of the register <2101H>.
The combination of this 4K-WORD and the 4K-WORD remaining will be determined by "OBJ NAME BASE SELEC of the register <2101H>.

OBJ Name Select

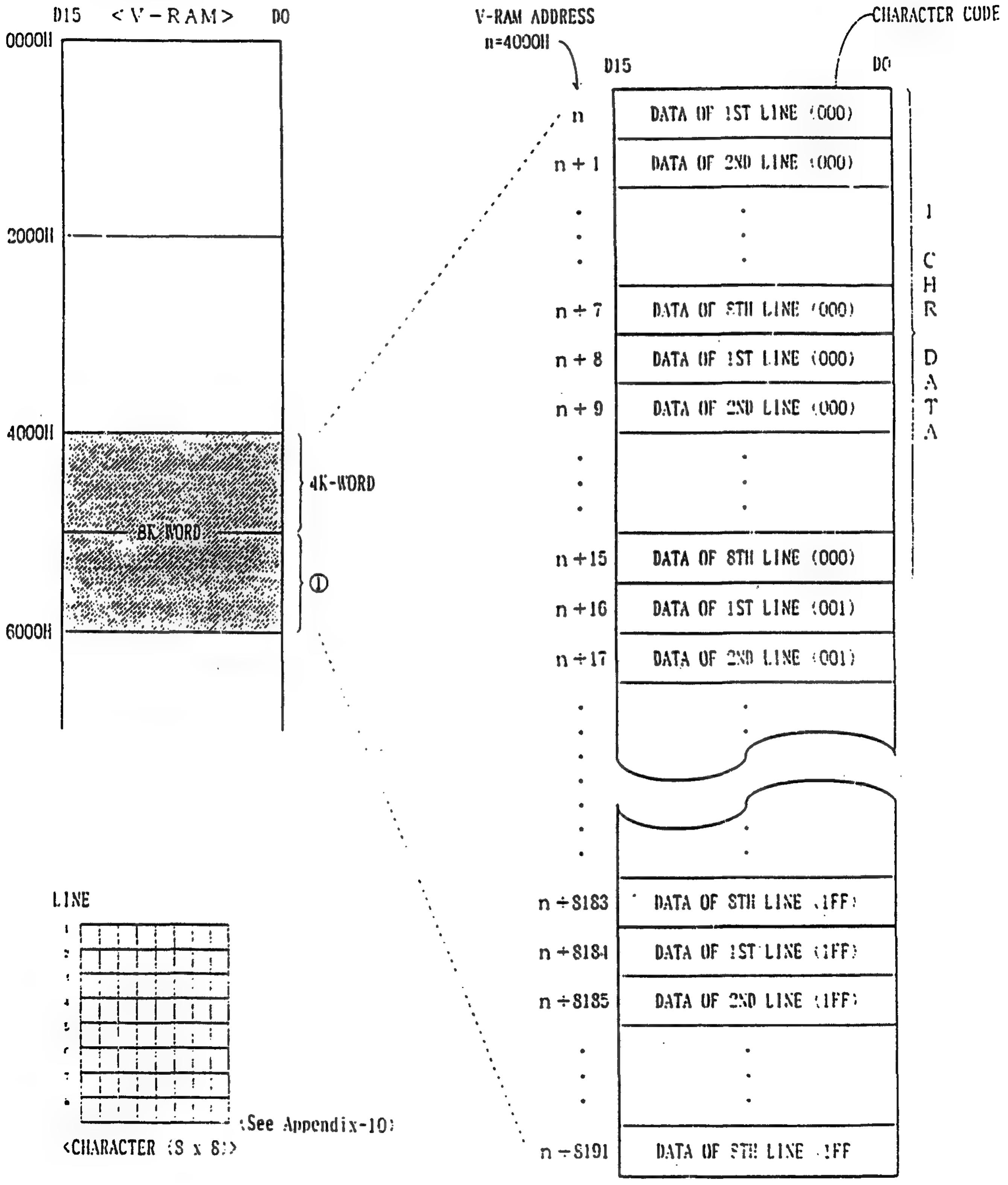
N1	N0	COMBINATION
0	0	4K-WORD - ①
0	1	4K-WORD - ②
1	0	4K-WORD - ③
1	1	4K-WORD - ④

OBJECT DATA TO BE STORED

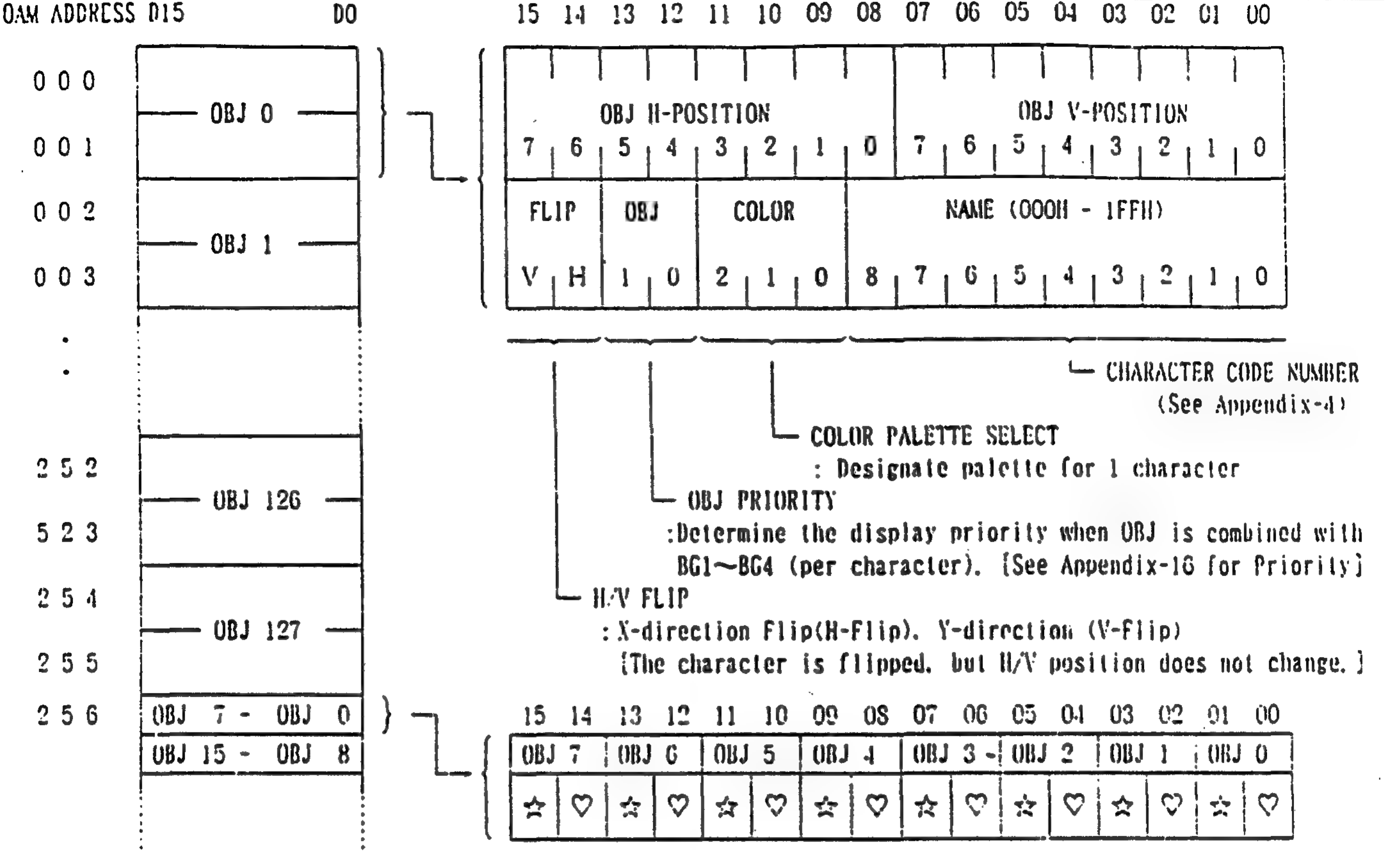
4 BIT CONSTRUCTION [8 x 8 x 4 Bit (16 WORD)/Character] (See Appendix-10)

8 x 8 (Character Size) x 4 (Bit Construction) x 512 (Number of character) ———— 16K-BYTE

[In case BA1=1 and BA0=0 are set by "OBJ NAME BASE ADDRESS" and also N1=0 and N0=0 are set by "OBJ NAME SELECT"]



OBJECT DATA



15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OBJ H-POSITION								OBJ V-POSITION							
7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
FLIP		OBJ		COLOR			NAME (000H - 1FFH)								
V	H	1	0	2	1	0	8	7	6	5	4	3	2	1	0

└ CHARACTER CODE NUMBER (See Appendix-4)

└ COLOR PALETTE SELECT
: Designate palette for 1 character

└ OBJ PRIORITY
:Determine the display priority when OBJ is combined with BG1~BG4 (per character). [See Appendix-16 for Priority]

└ H/V FLIP
:X-direction Flip(H-Flip). Y-direction (V-Flip)
[The character is flipped, but H/V position does not change.]

15	14	13	12	11	10	09	08	07	06	05	04	03	02	01	00
OBJ 7		OBJ 6		OBJ 5		OBJ 4		OBJ 3		OBJ 2		OBJ 1		OBJ 0	
☆	♡	☆	♡	☆	♡	☆	♡	☆	♡	☆	♡	☆	♡	☆	♡

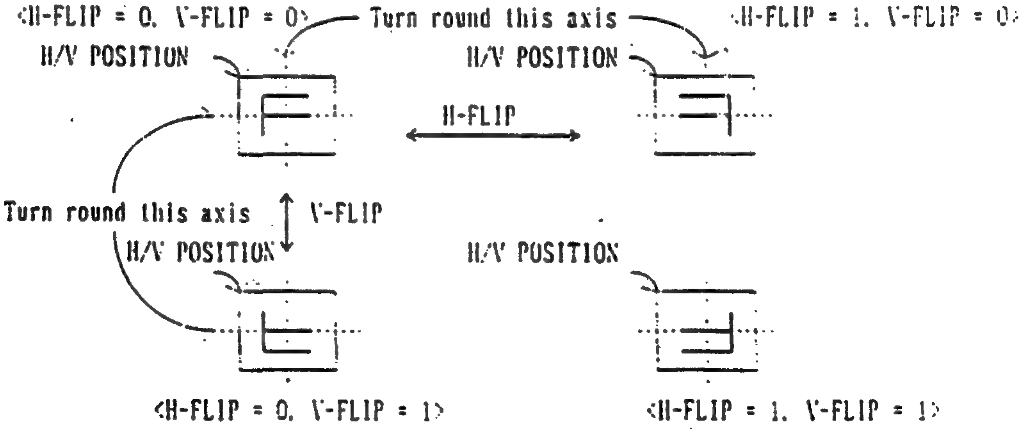
☆ Size large/Small ♡ H-Position MSB

The base position of the OBJ on the H-direction will be determined by both H-position (8-bit) and the H-position MSB.

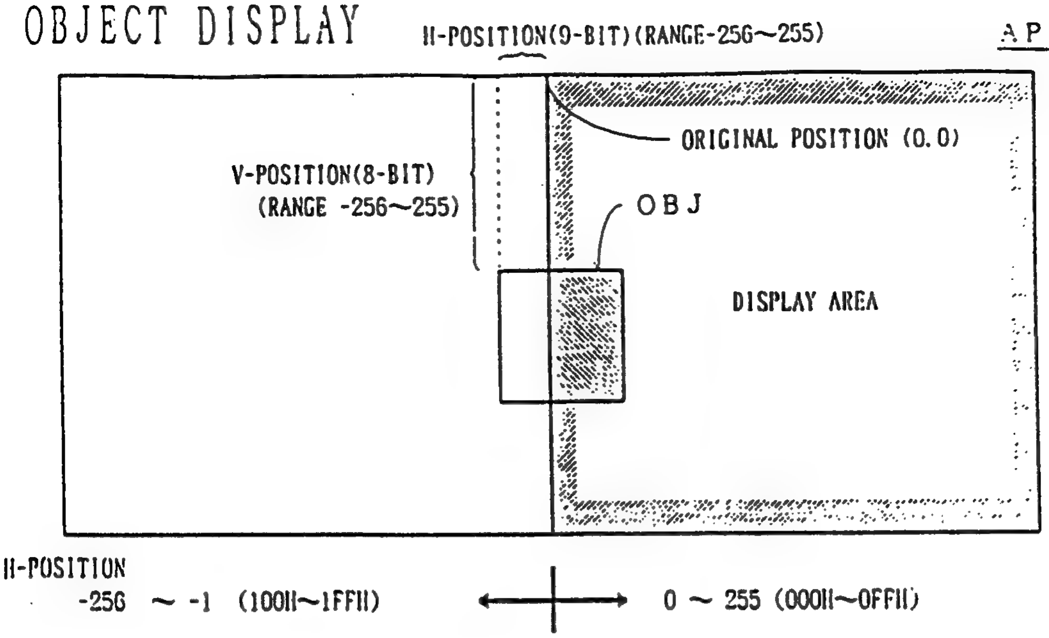
SIZE LARGE/SMALL: Determine the size to be used either of 2 OBJs selected by the register <2101H>.

┌ 0 : Select small size
└ 1 : Select large size

H/V FLIP



OBJECT DISPLAY

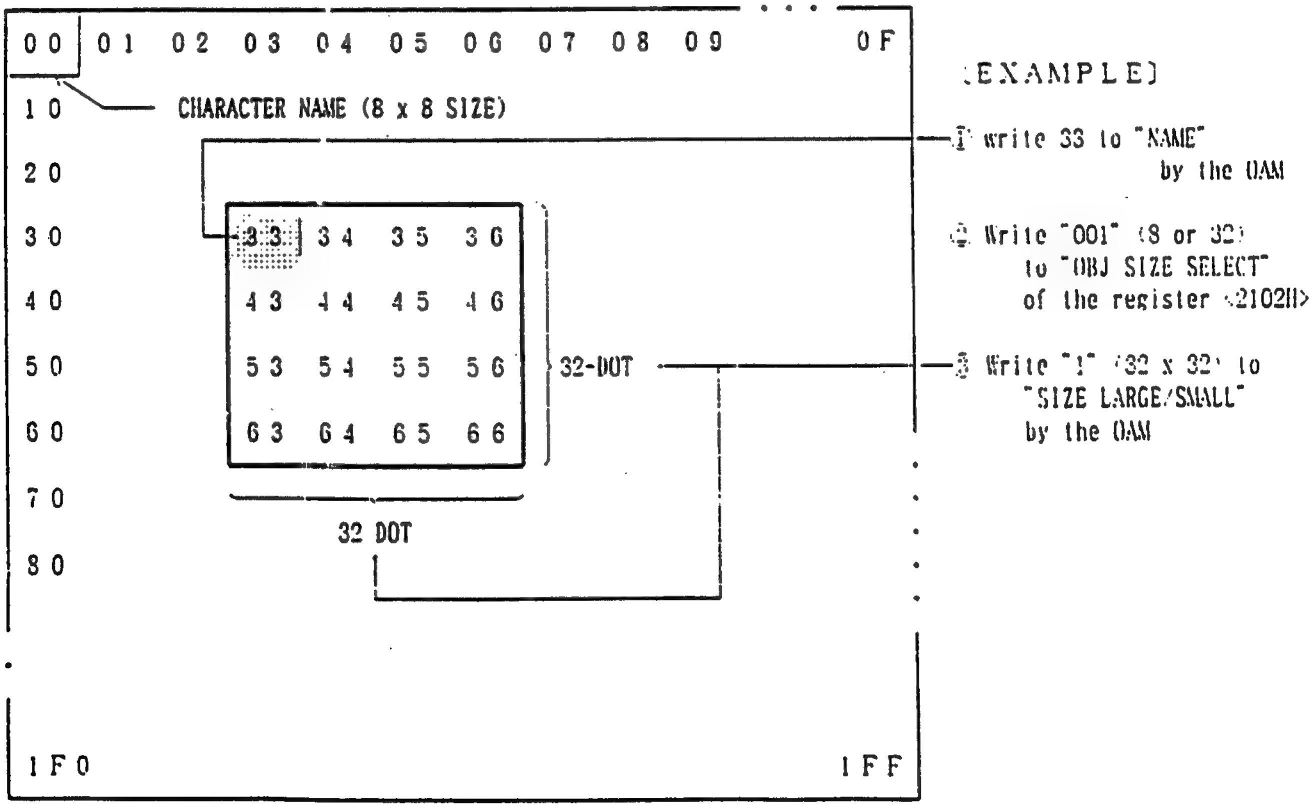


(NOTE-1) The H-position is a complementary expression of 2 (9-bit).

(NOTE-2) The coordinate of the OBJ displayed is shifted down compared to the coordinate of the BG displayed. [Interlace : 2-dot / Non-Interlace : 1-dot] (See Appendix-8)

(NOTE-3) "001H" is basically prohibited to use for 9-bit of the H-Position. (If it is used, it must be counted as OBJ quantity displayed even it is not displayed on the screen.)

OBJECT CHARACTER DATA CONSTRUCTION (V-RAM)


00 01 02 03 04 05 06 07 08 09 0F
10
CHARACTER NAME (8 x 8 SIZE)
20
30
33 34 35 36
40
43 44 45 46
50
53 54 55 56
60
63 64 65 66
70
80
1F0
1FF
32-DOT
32 DOT
[EXAMPLE]
① write 33 to "NAME" by the OAM
② Write "001" (8 or 32) to "OBJ SIZE SELECT" of the register <2102H>
③ Write "1" (32 x 32) to "SIZE LARGE/SMALL" by the OAM

In case the character code is 000 through 0FF, the V-RAM address per character data (16-word) will be "n(Name Base Address) + N(name) x 16 ~ n + N x 16 + 15" And In case the character code is 100 through 1FF, it will be "n + N_S (Name Select) x 4K + N x 16 ~ n + N_S x 4K + N x 16 + 15"

OBJECT MODE

# OF CELLS DISPLAYED	128			
CELL SIZE	8 × 8	16×16	32×32	64×64
# OF LINES DISPLAYED	32-pcs (converted to 8x8 size)			
# OF CELL-COLOR	16			
# OF PALETTE	8			
# OF COLOR ON SCREEN	128			
ATTRIBUTE	H-FLIP. V-FLIP FUNCTION DISPLAY PRIORITY (Select priority against BG)			

BG MODE

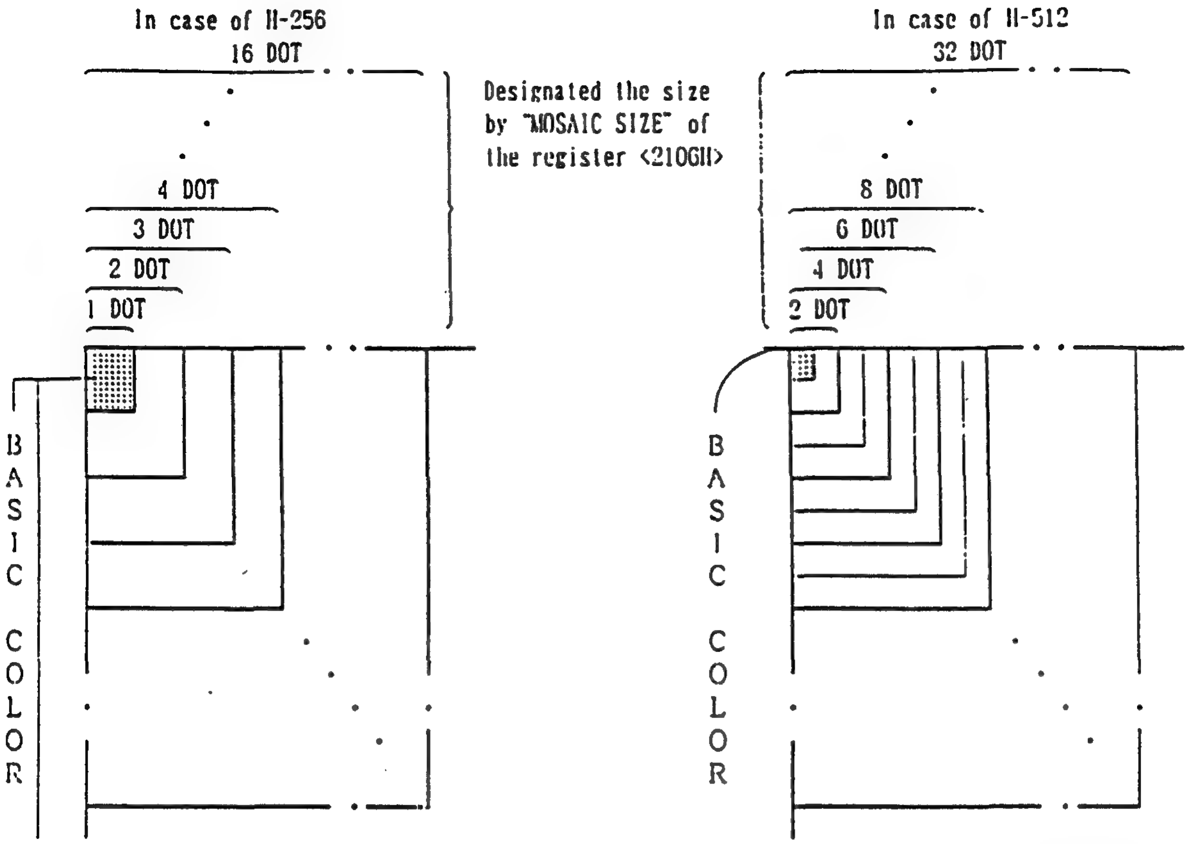
MODE	# OF SCREEN DISPLAYED	SCREEN	# OF CELL DOT	# OF CELL COLOR	# OF PALETTES	# OF COLORS PER SCREEN	FUNCTION
0	MAX 4	BG 1	8 × 8 & 16 × 16	4	8	32	H/V SCROLL H-FLIP. V-FLIP WINDOW MOSAIC FIXED-COLOR ADDITION SCREEN COLOR ADDITION
		BG 2		4	8	32	
		BG 3		4	8	32	
		BG 4		4	8	32	
1	MAX 3	BG 1		16	8	128	
		BG 2		16	8	128	
		BG 3		4	8	32	
2	MAX 2	BG 1		16	8	128	①
		BG 2		16	8	128	
3	MAX 2	BG 1		256	1	256	
		BG 2		16	8	128	
4	MAX 2	BG 1		256	1	256	①
		BG 2		4	8	32	
5	MAX 2	BG 1		16	8	128	②
		BG 2		4	8	32	
6	1	BG 1		16	8	128	①②
7	1	BG 1	8 × 8	256	1	256	③

① Offset value can be set in H/V direction against the cell

② H-512 mode vertical expansion caused interlace

③ Enlargement Reduction Rotation

MOSAIC SCREEN

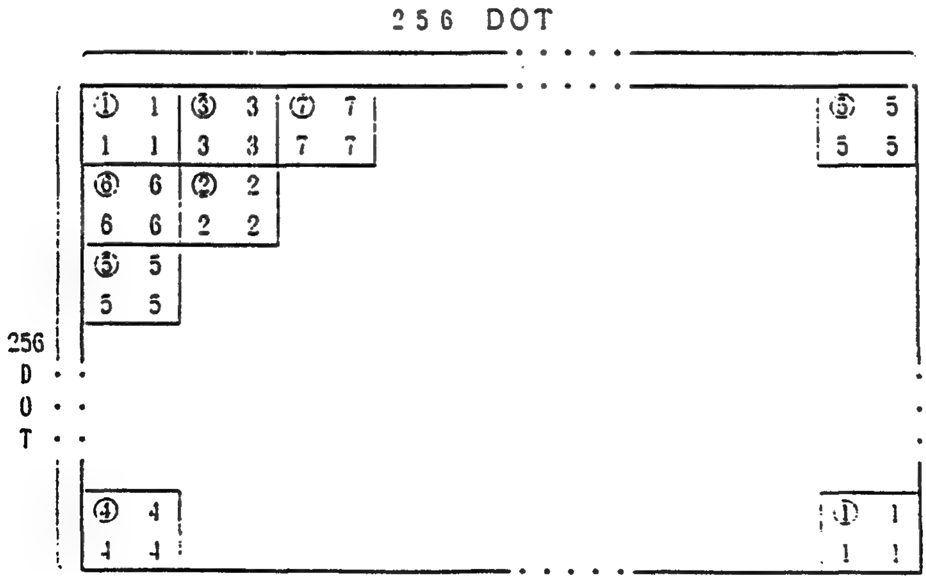


*all dots of the size designated become this color.

In case of the H-Pseudo 512 mode. 2 x 2-dot mosaic can be made in size-0. (See No. 3)

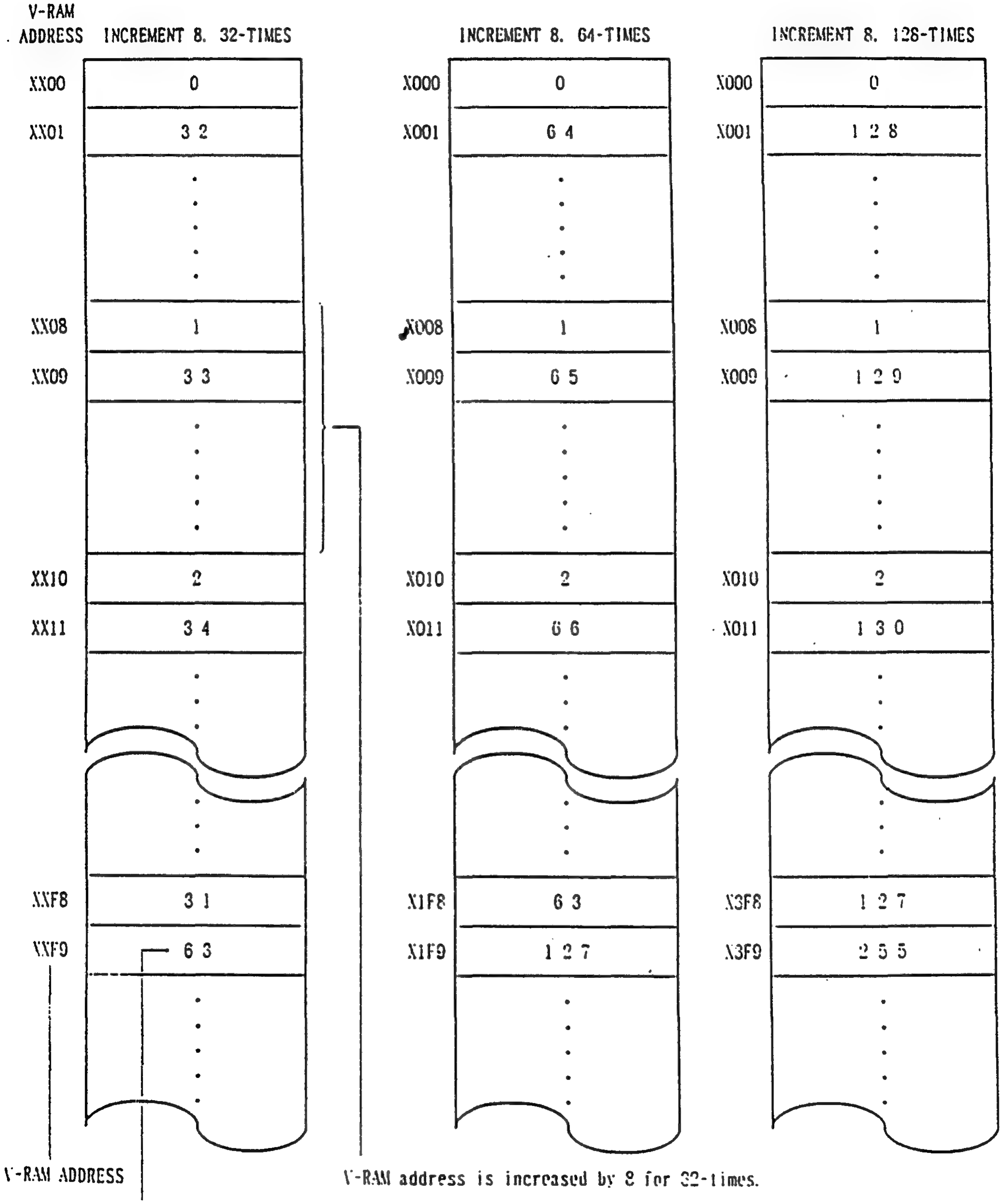
MOSAIC SCREEN DISPLAY EXAMPLE (BG SCREEN)

(When the mosaic size is 2x2-dot in the 256-mode)



○ is the basic color data

ADDRESS INCREMENT VALUE SET (THE ORDER OF ACCESSING)



V-RAM ADDRESS

V-RAM address is increased by 8 for 32-times.

ORDER OF ACCESS (corresponding to the address designated by the register <2116H>~<2117H>)

BG SC DATA (MODE 0~6)

D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0
FLIP		BG	COLOR			NAME (000H~3FFH)									
V	H	Pri.	2	1	0	9	8	7	6	5	4	3	2	1	0

CHARACTER CODE NUMBER

COLOR PALETTE SELECT : PALETTE DESIGNATION PER CHARACTER <8-Palettes>

BG PRIORITY : Determine the display priority per character in case OBJ and BG1 ~BG4 are combined on the same screen.

H/V FLIP : X-Directional Flip (H-FLIP), Y-Directional Flip (V-FLIP)

BG SCREEN H/V SCROLL

- RANGE OF H-SCROLL
  0 ~ 1024 DOT
- RANGE OF V-SCROLL
  0 ~ 1024 DOT

H/V scroll range may be changed and 2-dot scroll may be possible, depending on the combination of the modes (512, 16-size, interlace etc.).
Also, SC size may be changed against the screen. (See Appendix-18 & 19)

REGISTER <210DH><210FH>
<2111H><2113H>

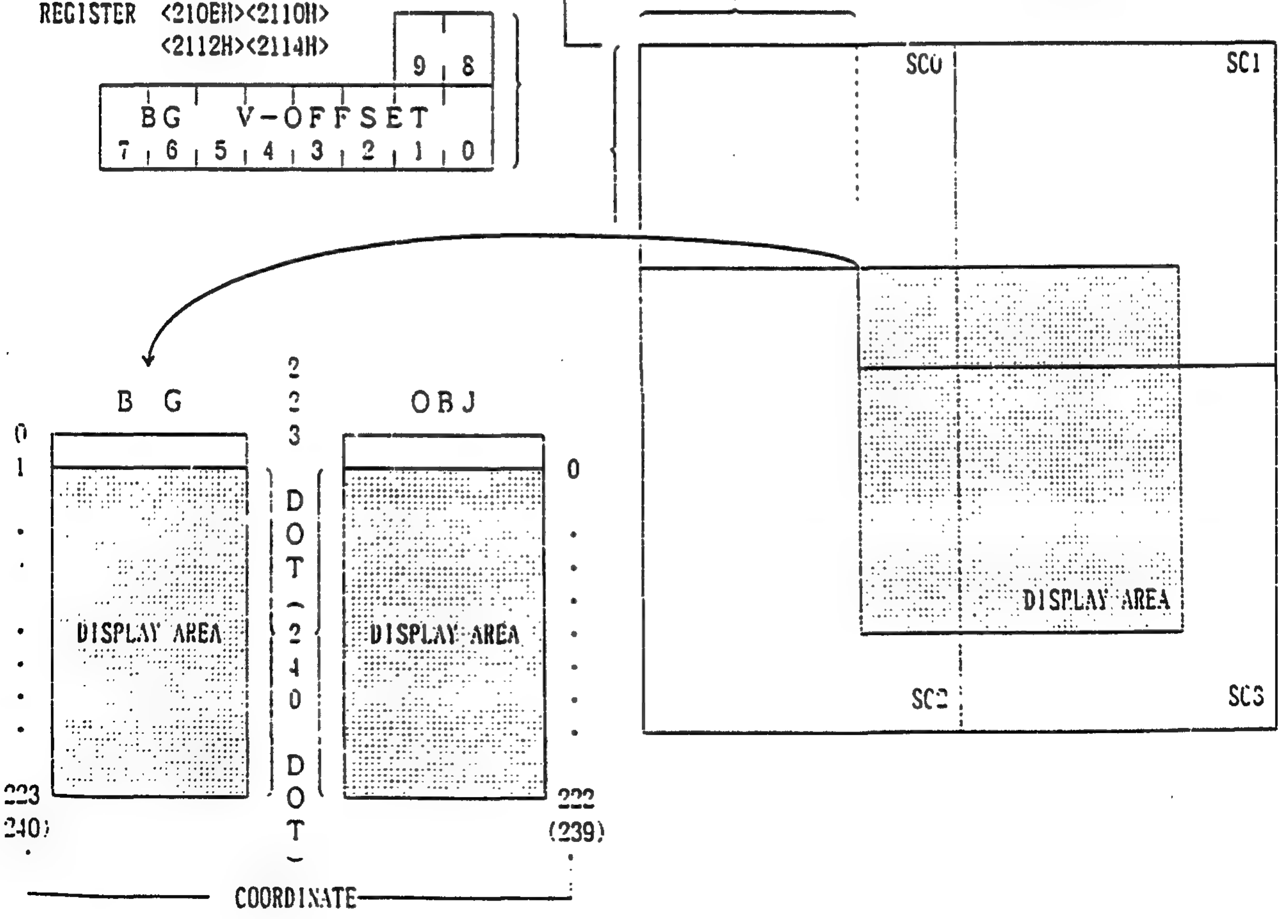
9	8

BG H-OFFSET							
7	6	5	4	3	2	1	0

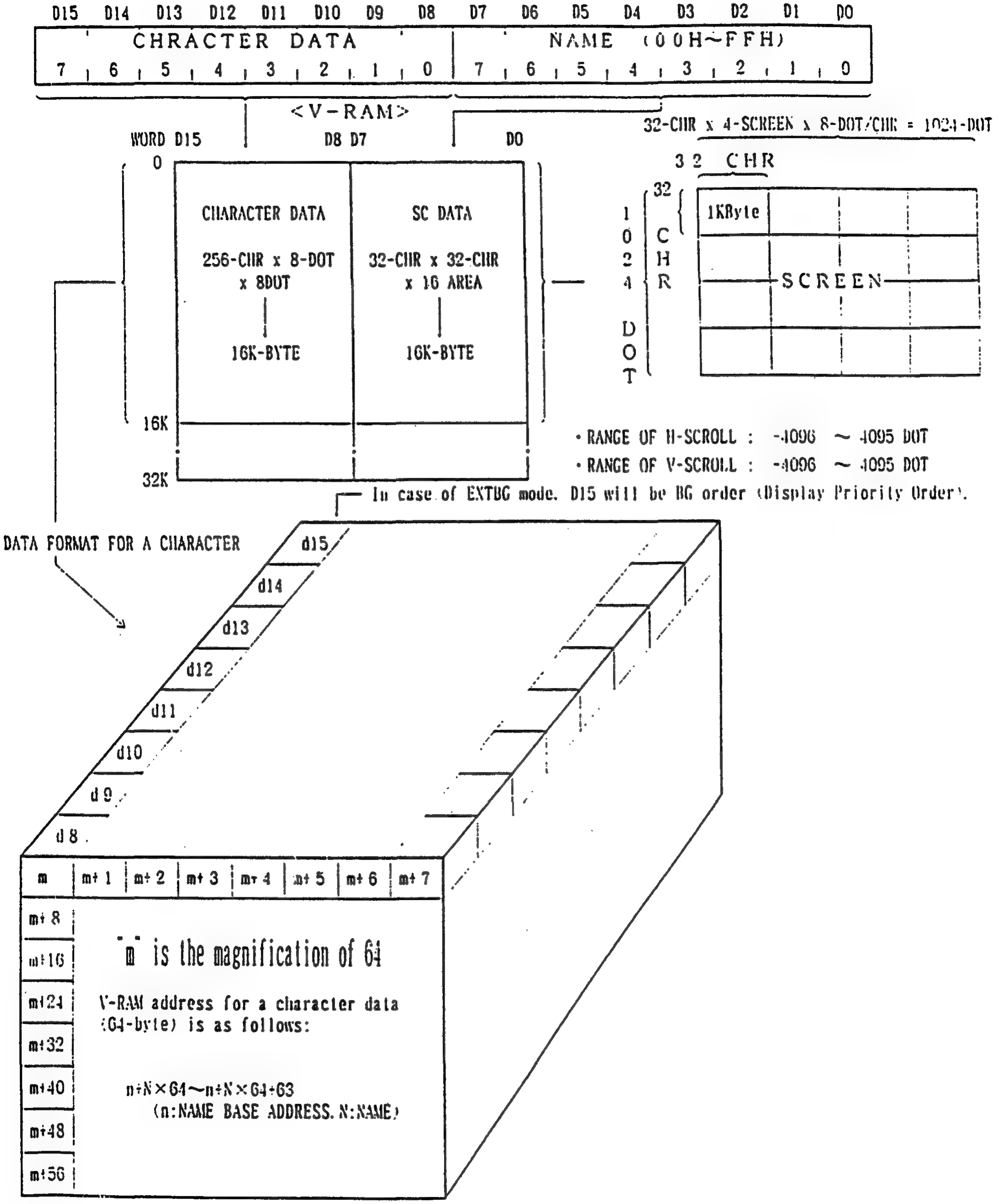
REGISTER <210EH><2110H>
<2112H><2114H>

9	8

BG V-OFFSET							
7	6	5	4	3	2	1	0



BG SC DATA (MODE 7)



32-CHR x 4-SCREEN x 8-DOT/CHR = 1024-DOT

- RANGE OF H-SCROLL : -4096 ~ 4095 DOT
- RANGE OF V-SCROLL : -4096 ~ 4095 DOT

In case of EXTBG mode, D15 will be BG order (Display Priority Order).

"m" is the magnification of 64

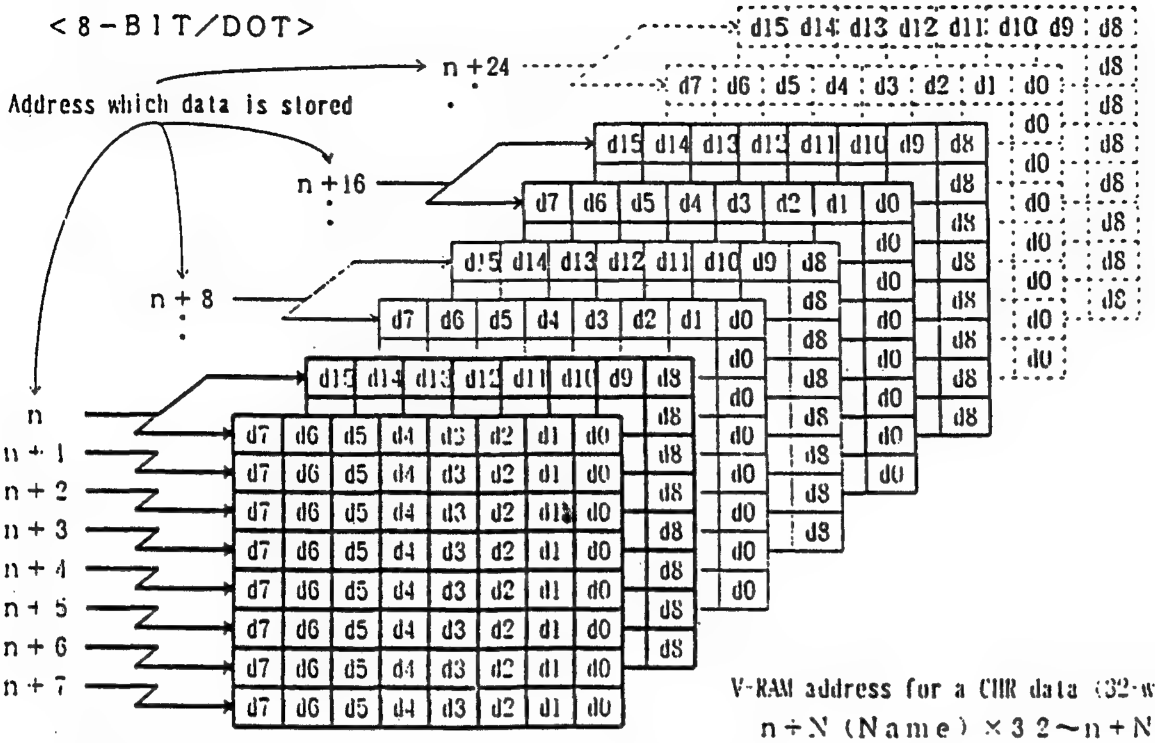
V-RAM address for a character data (64-byte) is as follows:

n+N×64~n+N×64+63
(n:NAME BASE ADDRESS, N:NAME)

CHR DATA CONSTRUCTION

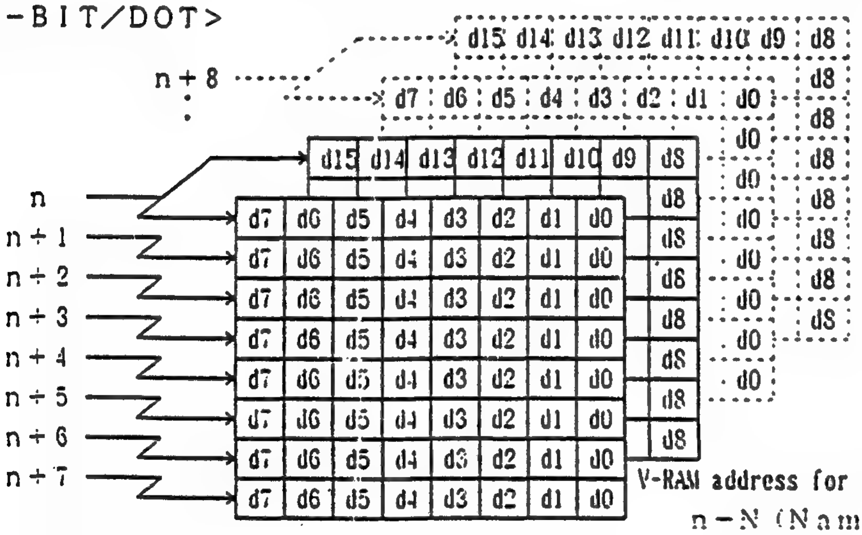
※ n : Name Base Address

<8-BIT/DOT>



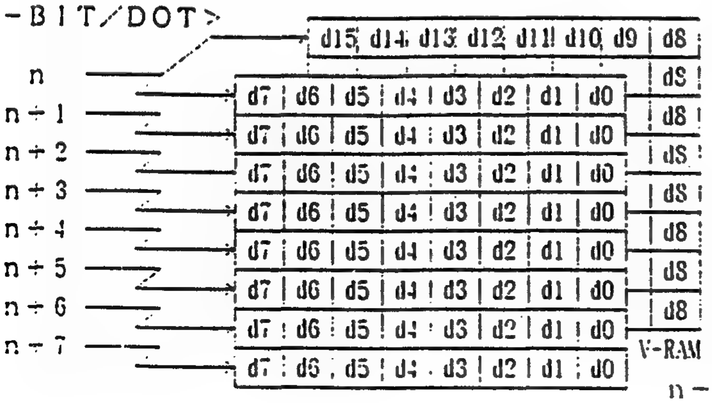
V-RAM address for a CHR data (32-word) is as follows:
n + N (Name) × 32 ~ n + N × 32 + 31

<4-BIT/DOT>



V-RAM address for a CHR data (16-word) is as follows:
n + N (Name) × 16 ~ n + N × 16 + 15

<2-BIT/DOT>



V-RAM address for a CHR data (8-word) is as follows:
n + N (Name) × 8 ~ n + N × 8 + 7

OFFSET CHANGE MODE

The offset change mode can be used in the BG mode 2, 4 and 6, and the following data is required in this mode.

d15	d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0
H/V	BG 2 EN	BG 1 EN				OFFSET DATA									

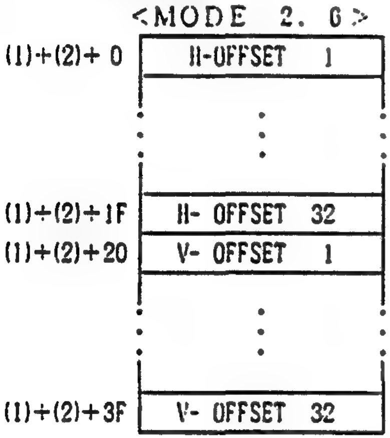
└─ H.V OFFSET VALUE (in the change mode)

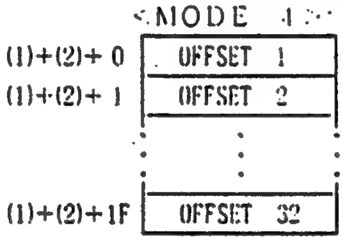
In case of the H-OFFSET, the data (D0 ~D2) will be invalid.
In case of the character (16 x 16), "D3" is effective every 3rd.

OFFSET MODE ENABLE
- 0 : Disable
- 1 : Enable

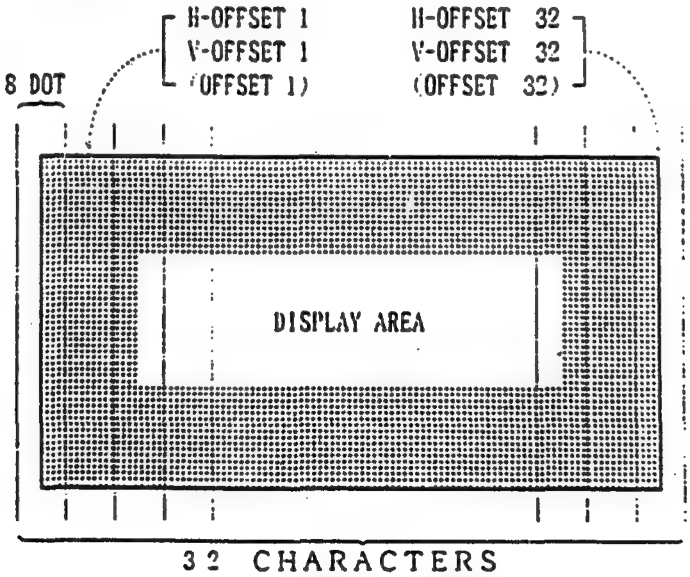
Designate either H-OFFSET or V-OFFSET for the OFFSET data d0 ~d9. (Only BG MODE 4 is effective)
- 0 : H-OFFSET
- 1 : V-OFFSET

This data should be written to the address, which is designated by "BG3 SC BASE ADDRESS" of register <2109H>, using the mode designated. (See below)





In case BG3 SC size is S1=0, S0=0
(1) : BG3 SC Base Address ([value set by "d2"~"d7" of <2109H>]×1024)
(2) : BG3 SC Offset Address ([value set by "d3"~"d7" of <2112H>]×32
+ ([value set by "d3"~"d7" of <2111H>])



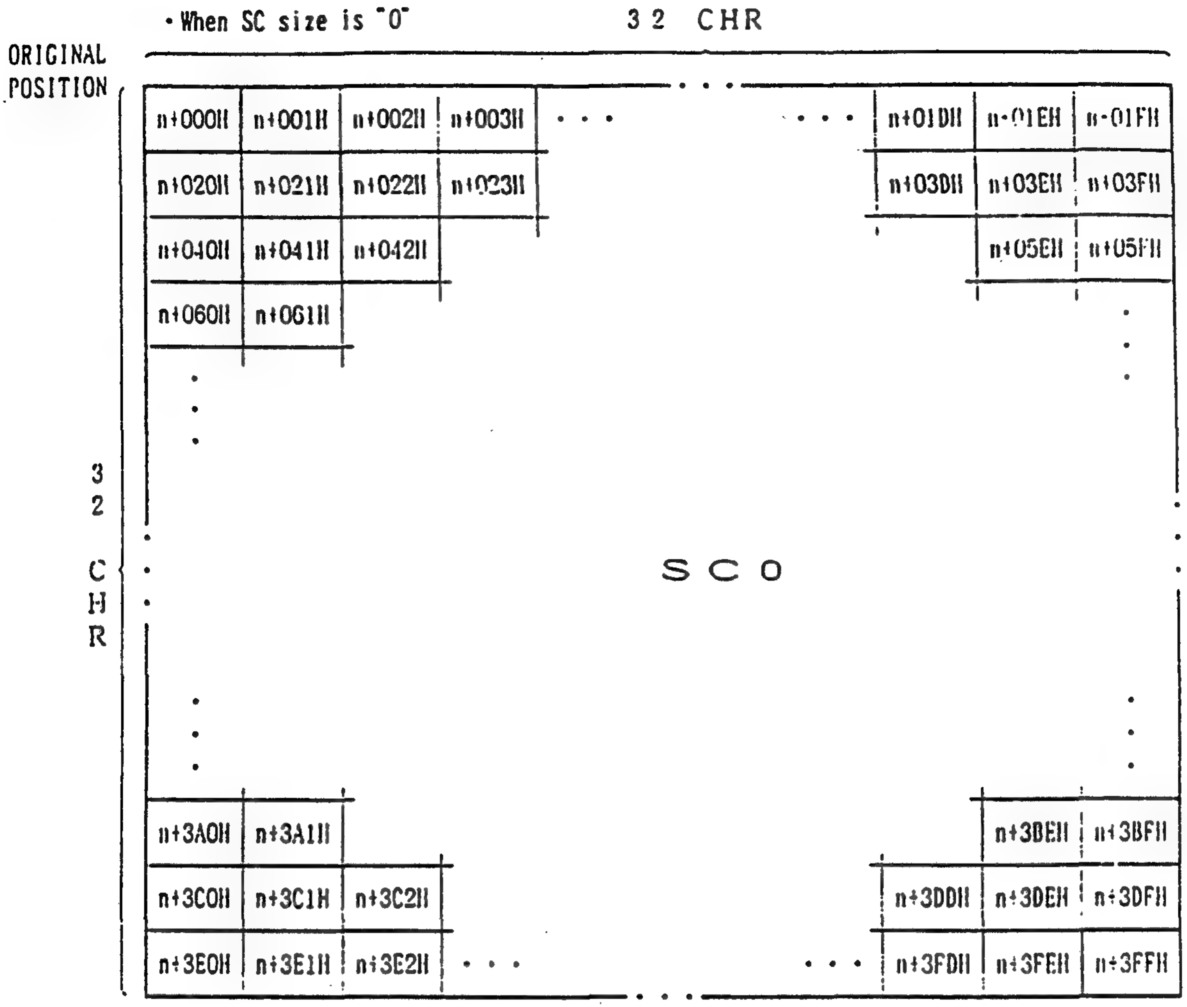
The offset value can be changed by each column (character unit).

・Up to 3rd character can be seen horizontally on the screen by setting the offset value of the entire screen, but the offset can not be changed for 1st character (0 character).

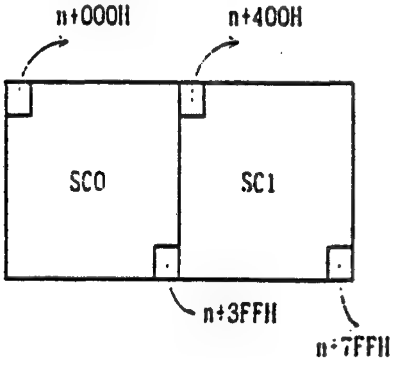
BG SCREEN

(n=SC Base Address(6-BIT)× 400H)

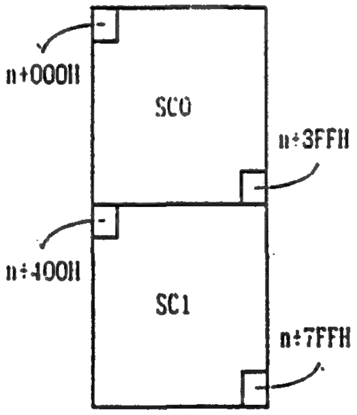
• When SC size is "0"



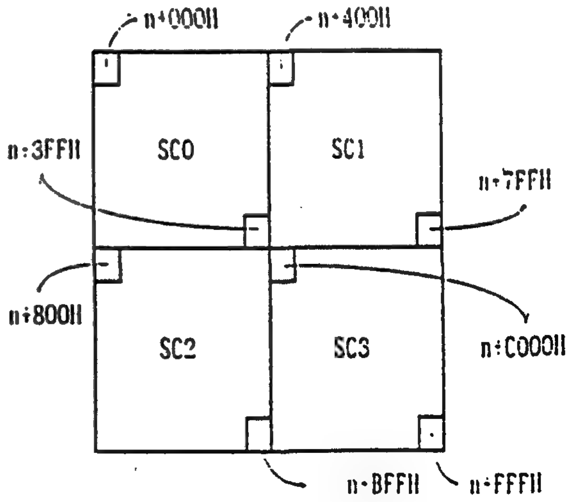
• When SC size is "1"



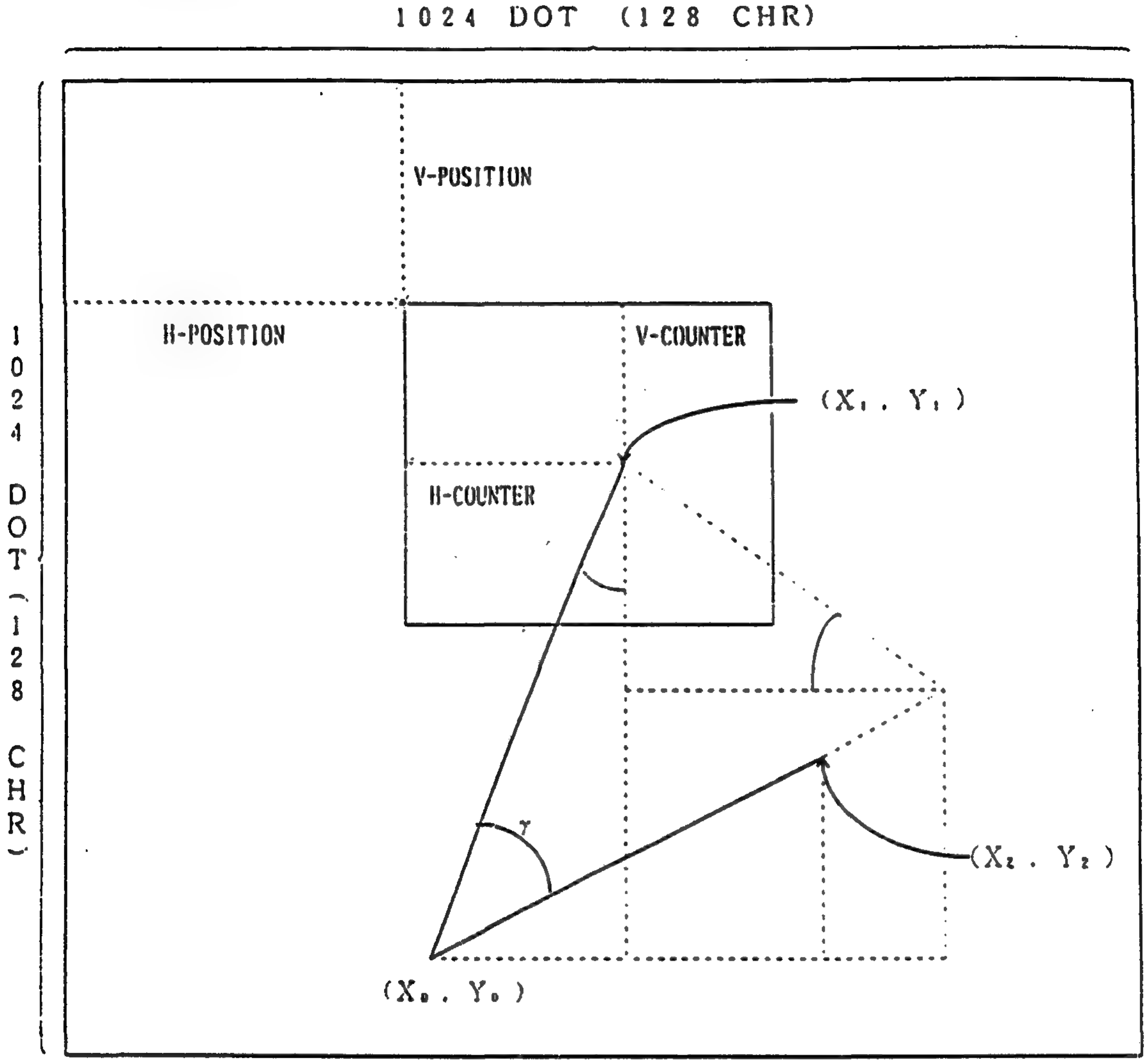
• When SC size is "2"



• When SC size is "3"



OPERATION (ROTATION/ENLARGEMENT/REDUCTION)



ROTATIONAL TRANSFORM FORMULA

$$\begin{bmatrix} X_2 \\ Y_2 \end{bmatrix} = \begin{bmatrix} \cos\gamma & \sin\gamma \\ -\sin\gamma & \cos\gamma \end{bmatrix} \begin{bmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{bmatrix} + \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix}$$

$X_0 \cdot Y_0$: Center Coordinate $\quad$ $X_1 \cdot Y_1$: Display Coordinate

$X_2 \cdot Y_2$: Coordinate before calculation of display coordinate

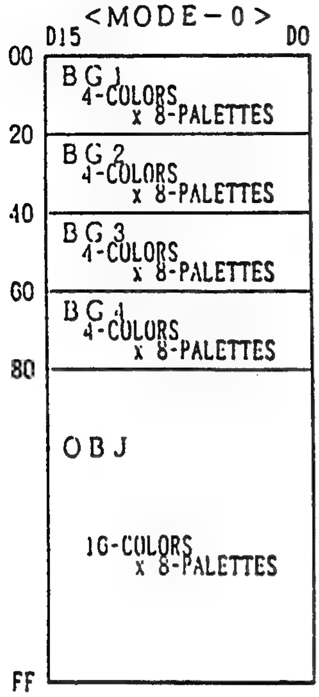
If the reduction rates for X-dir (α) and the reduction rates for Y-dir (β) are considered, the formula described above will be as follows :

$$\begin{bmatrix} X_2 \\ Y_2 \end{bmatrix} = \begin{bmatrix} A & B \\ C & D \end{bmatrix} \begin{bmatrix} X_1 - X_0 \\ Y_1 - Y_0 \end{bmatrix} + \begin{bmatrix} X_0 \\ Y_0 \end{bmatrix}$$

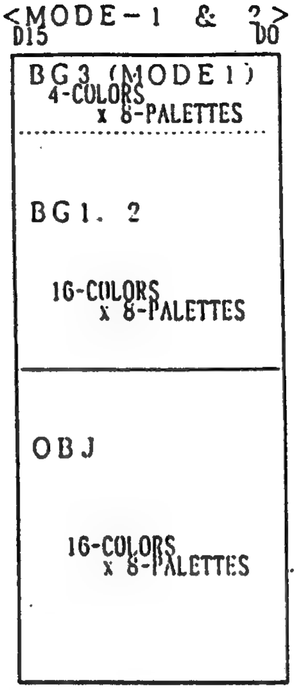
$A = \cos\gamma \times (1/\alpha)$, $\quad B = \sin\gamma \times (1/\alpha)$

$C = -\sin\gamma \times (1/\beta)$, $\quad D = \cos\gamma \times (1/\beta)$

CG-RAM



- 4-Screens for BG

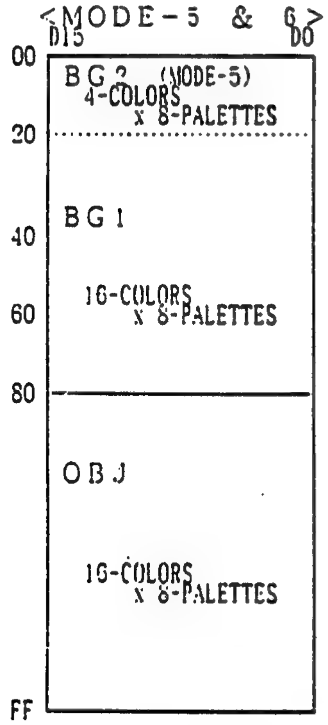


<MODE-1>

- 3-Screens for BG
- BG1 & 2 color data are held in common in the range of 0~7F
- BG3 color data are held in common in the range of 0~1F

<MODE-2>

- 2-Screens for BG
- BG1 & 2 color data are held in common in the range of 0~7F

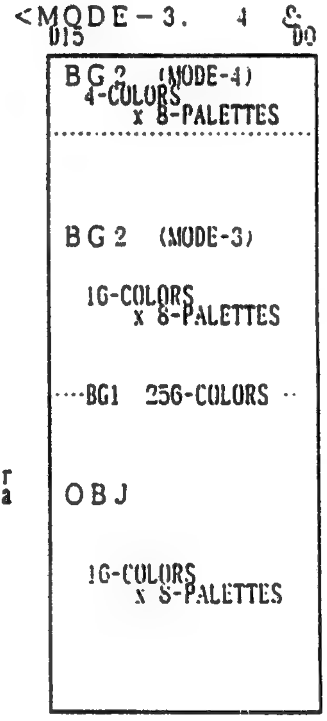


<MODE-5>

- 2-Screens for BG
- BG1 & 2 color data are held in common in the range of 0~1F

<MODE-6>

- 1-Screen for BG
- 0~7F are used just for BG1 color data



<MODE-3>

- 2-Screens for BG
- BG2 color data are held in common in the range of 0~7F (CG Direct select is excluded)

<MODE-4>

- 2-Screens for BG
- BG2 color data are in commo in the range of 0~1F. (CG Direct select is excluded.

<MODE-7>

- 1-Screen for BG (CG Direct select is excluded)

<EXTBG ON MODE-7>

- 1-Screen for BG
- 0~7F are used just for BG2 color data

※OBJ is held in common with BG-1.

CG-RAM COLOR DATA

BLUE					GREEN					RED				
d14	d13	d12	d11	d10	d9	d8	d7	d6	d5	d4	d3	d2	d1	d0

DIRECT SELECT COLOR DATA

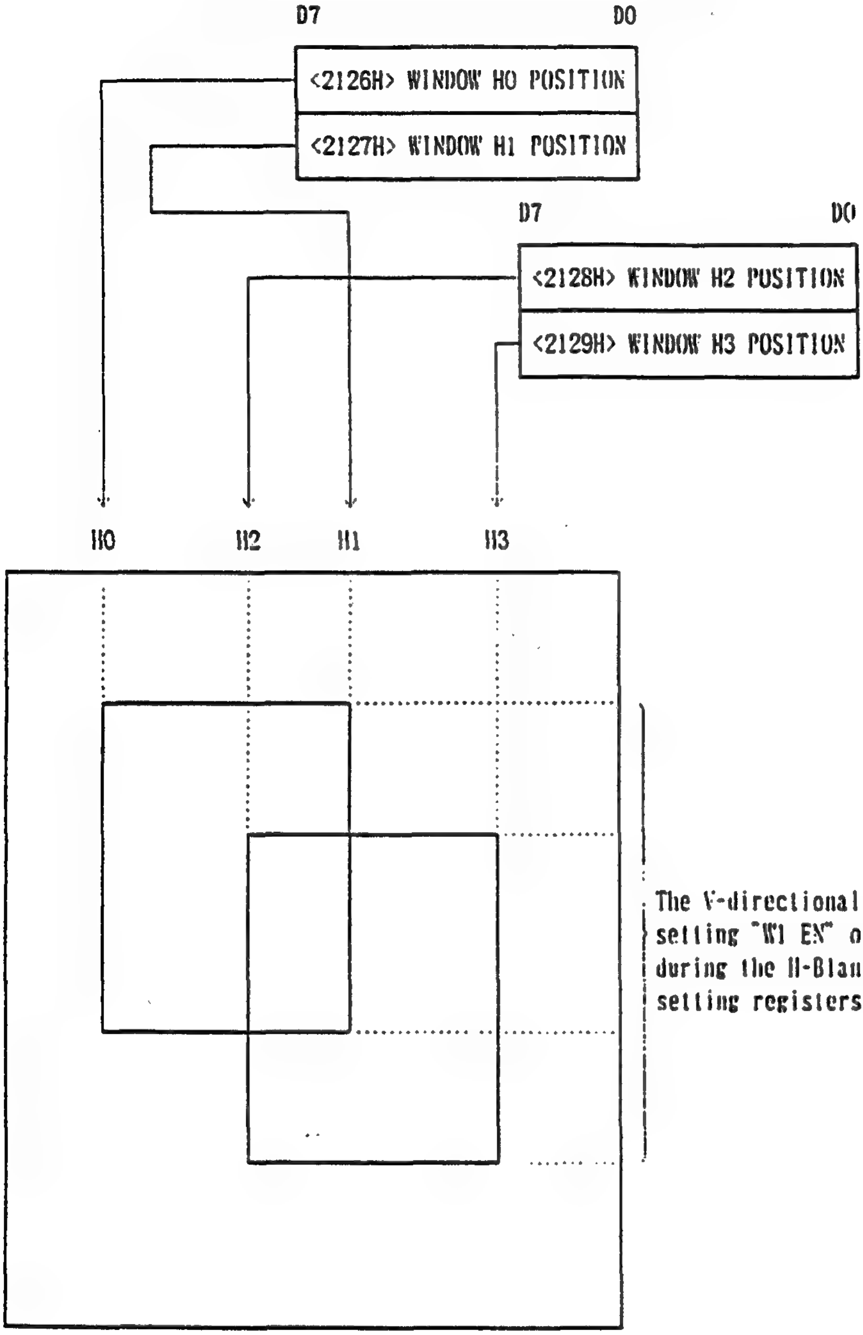
BLUE					GREEN					RED				
DA7	DA6	CL2	0	0	DA5	DA4	DA3	CL1	0	DA2	DA1	DA0	CL0	0

NOTE : DA0~DA7 are used for the character dot data. CL0~CL2 are used for the BG-SC data of the color. (However, in case of Mode-7, CL0 ~CL2 should be "0".)

NOTE : If they are "0", it becomes transparent. The color of CG-RAM address (00H) will be background.

WINDOW

REGISTER<2126H>~<2129H>

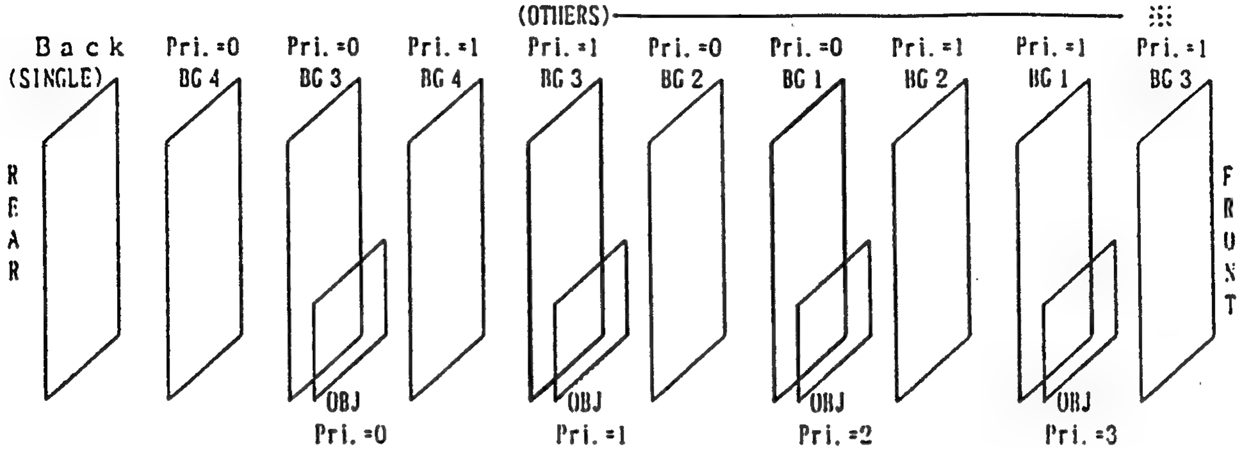

D7
D0
<2126H> WINDOW H0 POSITION
<2127H> WINDOW H1 POSITION
D7
D0
<2128H> WINDOW H2 POSITION
<2129H> WINDOW H3 POSITION
H0
H2
H1
H3

The V-directional position is determined by setting "W1 EN" of registers <2123H><2124><2125H> during the H-Blank period or determined by setting registers <2126H> ~<2129H>.

BG & OBJ PRIORITY

4-SCREEN/3-SCREEN MODE

※ In case "D3=1" is selected by register <2105H> in the mode-1



<Example of Display Priority (in case of mode 0 & 4)>

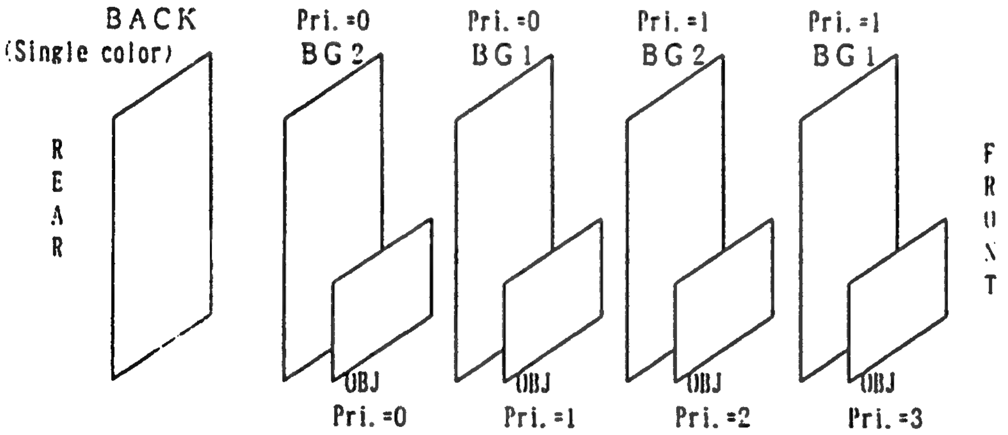
BG1 Pri.=0
BG2 Pri.=1
BG3 Pri.=0
BG4 Pri.=1
OBJ Pri.=2
are set ——— BG2-OBJ-BG1-BG4-BG3-Back

High Priority (FRONT) ——— Low Priority (REAR)

(Displayed in the order of above)

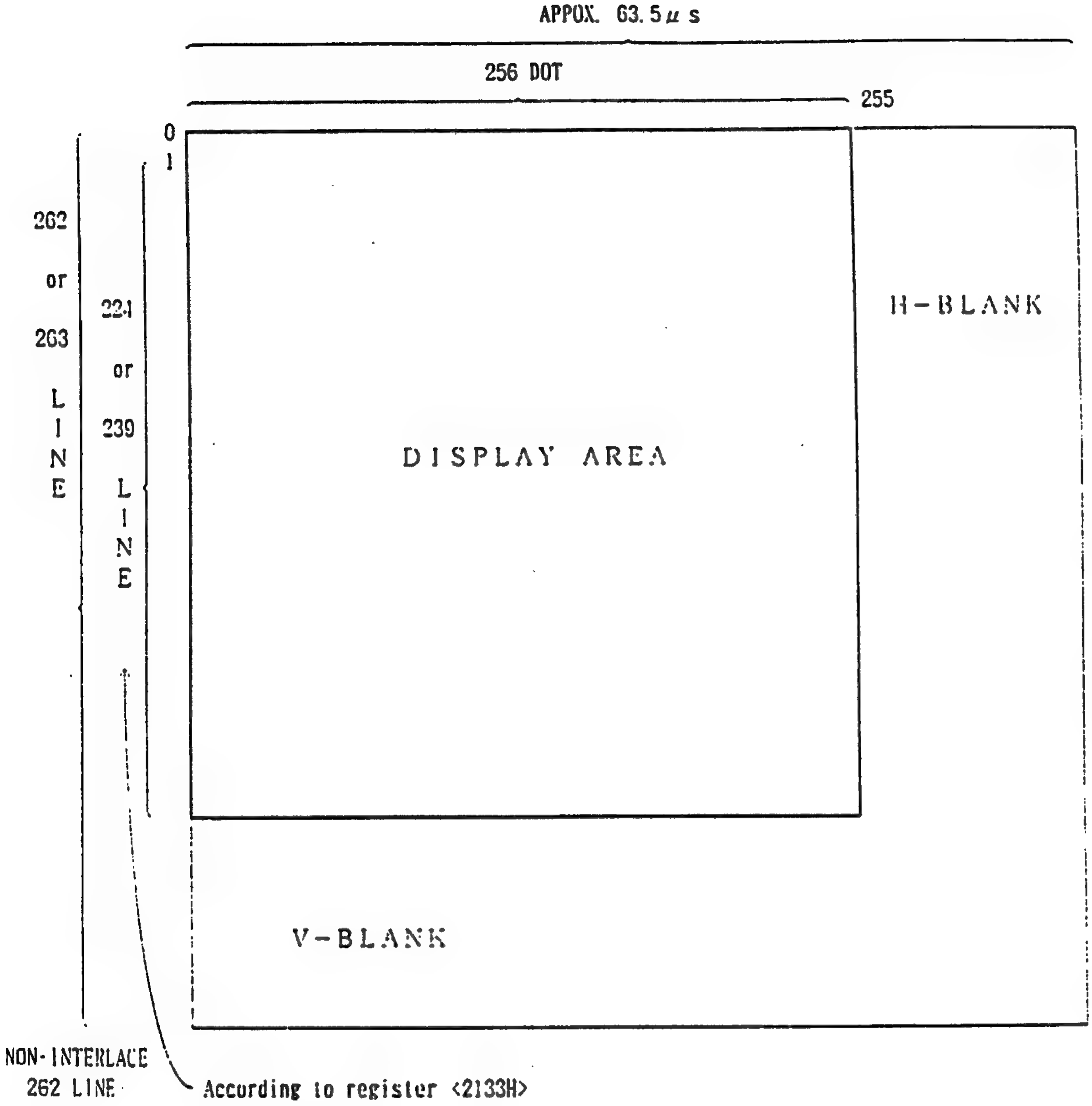
2-SCREEN/1-SCREEN MODE

(in case Mode 2~7 is selected by the register <2105H>)



NOTE : In case of the display priority between the OBJs, normally the lower numbered OBJ will be displayed as higher priority. (See Page-35 for exception)
This display priority will be determined before the priority between OBJ and BG is determined.

SCREEN

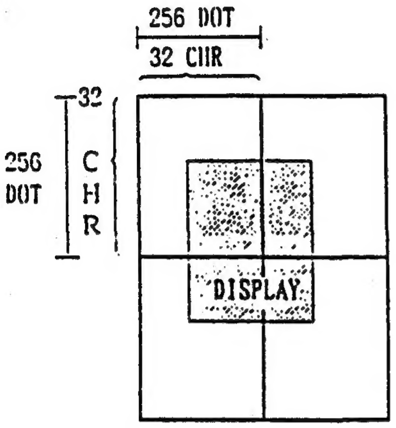

APPOX. 63.5μs
256 DOT
255
0
1
262
or
263
LINE
224
or
239
LINE
DISPLAY AREA
H-BLANK
V-BLANK
NON-INTERLACE
262 LINE
According to register <2133H>

BG SCREEN

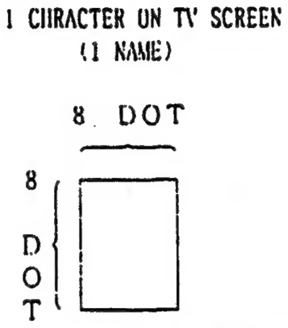
H/V SCROLL ① (Scroll range by the combination of modes. and SC size against screen)
<Example in case SC size is "3" (SEE NO.4)>

★In case of 0. 1. 2 & 4

・BG SIZE [8x8]



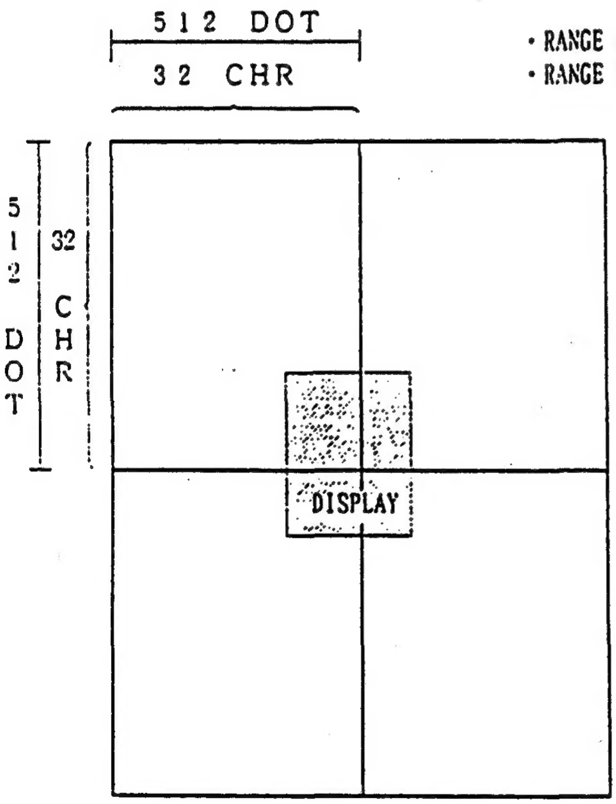
SC SCREEN

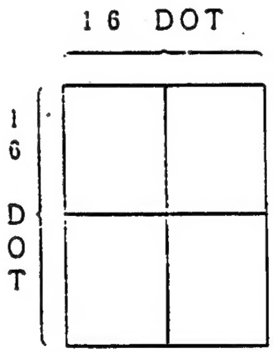


・RANGE OF H-SCROLL: 0~ 511 (Scroll 1-dot to the left by adding 1
・RANGE OF V-SCROLL: 0~ 511 (Scroll 1-dot to the up by adding 1

・BG SIZE [16x16]

・RANGE OF H-SCROLL: 0~ 1023 (Scroll 1-dot to the left by adding 1
・RANGE OF V-SCROLL: 0~ 1023 (Scroll 1-dot to the up by adding 1)



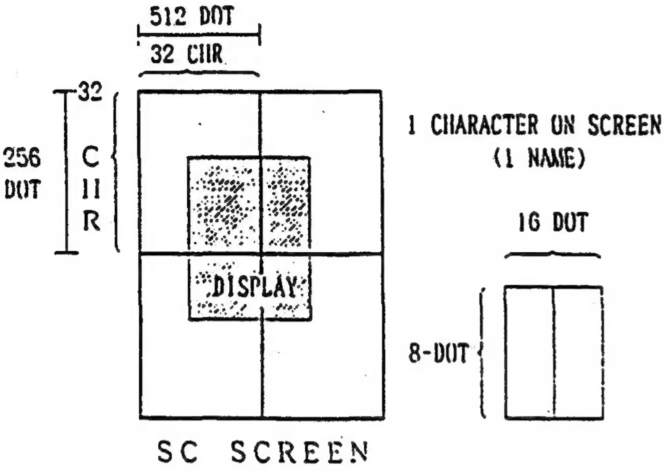


BG SCREEN

H/V SCROLL ② (Scroll range by the combination of modes, and SC size against screen)
<Example in case SC size is "3" (SEE NO.4)>

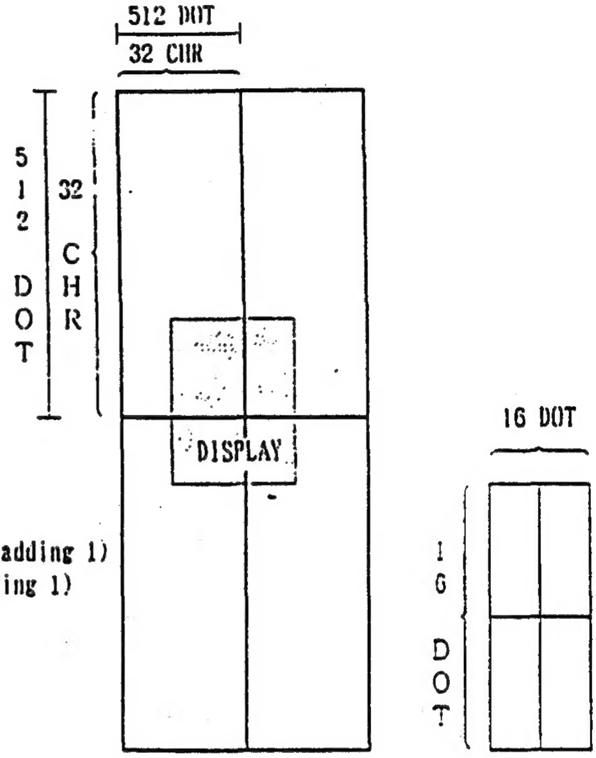
★IN CASE OF MODE-5, MODE-6 & NON-INTERLACE

- BG SIZE [8 x 8]



- RANGE OF H-SCROLL:0 ~ 511 (Scroll 2-dots to the left by adding 1)
- RANGE OF V-SCROLL:0 ~ 511 (Scroll 1-dot to the up by adding 1)

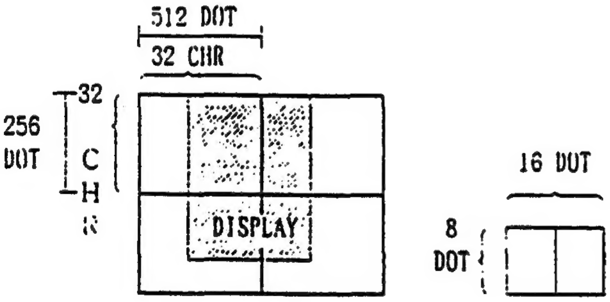
- BG SIZE [16 x 16]



- RANGE OF H-SCROLL: 0~ 511 (Scroll 2-dots to the left by adding 1)
- RANGE OF V-SCROLL: 0~ 1023 (Scroll 1-dot to the up by adding 1)

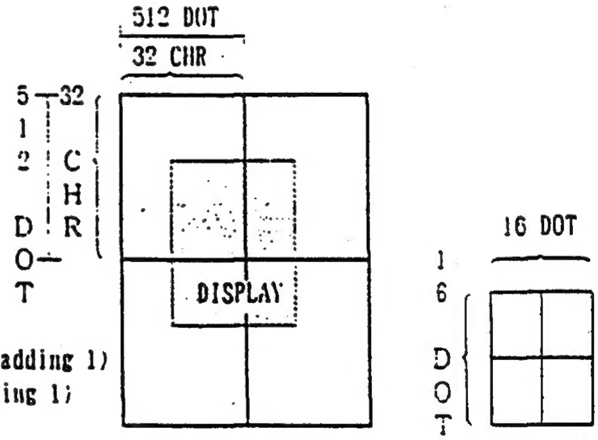
★IN CASE OF MODE-5 & 6, INTERLACE

- BG SIZE [8 x 8]

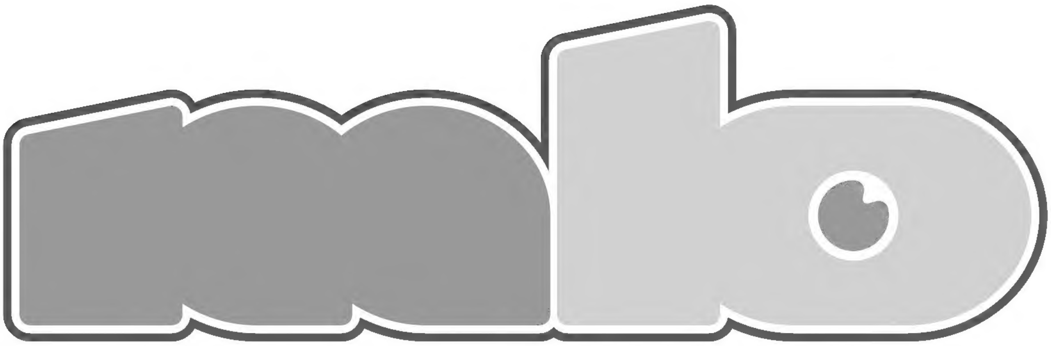


- RANGE OF H-SCROLL: 0~ 511 (Scroll 2-dots to the left by adding 1)
- RANGE OF V-SCROLL: 0~ 511 (Scroll 1-dot to the up by adding 1)

- BG SIZE [16 x 16]



- RANGE OF H-SCROLL: 0~ 511 (Scroll 2-dots to the left by adding 1)
- RANGE OF V-SCROLL: 0~ 1023 (Scroll 1-dot to the up by adding 1)



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